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TO
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on
Millimeter Wave Electronics

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13. ABSTRACT *(Maximum 200 words)*

This technical report summarizes activities of five (5) research units of UCLA JSEP during 1998 and serves as the Final Technical Report. The short length of the present research program is mainly dedicated to successful "close down" of the JSEP effort. By its nature, we have done the following: (1) We have tried to complete the technical project with graduate students completing their degree requirements. (2) Substantial effort has been expended to find out the method to transition the technical projects to industry and government agencies. (3) Extrapolation of the research effort has been used to initiate newly funded research projects. For instance, some of the JSEP findings are extended and included in some of the MURI programs at UCLA.

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Observation of new type resonances in triple barrier resonant tunneling diodes

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Current–voltage characteristics measured in triple barrier resonant tunneling diodes reveal new features about energy level alignment in a superlattice. Our data indicate that energy levels in the two quantum wells are not aligned at current peaks. Current peaks are observed when one of the energy levels in the two wells becomes resonant with the emitter level. One of the current peak was thermally activated, and showed inverted bistability at 77 K temperature. We explain that this is due to X state assisted tunneling. © *1997 American Institute of Physics.* [S0021-8979(97)04818-4]

I. INTRODUCTION

Since the original proposal of a superlattice structure by Esaki and Tsu,[1] there has been considerable interest in the transport properties of this structure. In a superlattice, current–voltage characteristics show multiple peaks due to nonuniform electric field distribution in the structure, which is called high field domain formation.[2,3] It was previously thought that the electric field in a superlattice always aligns the energy levels of the neighboring wells at the same height. However, Kwok *et al.* recently reported that the electric field in the high field domain is lower than the field for resonant alignment.[4] Their photoluminescence experiments showed that resonant alignment of energy levels occurred only for a narrow region of bias. It was explained that the nonresonant alignment is due to current conservation across the structure. Since the upper level current is much larger than the lower level current, resonant alignment is not allowed because of the current difference.

The details of energy level alignment by the applied electric field is not yet thoroughly understood. It was not easy to interpret superlattice current–voltage (I–V) data since there are many wells involved, where each well can give current peaks of a different nature. In order to simplify this problem, we studied the transport properties of triple barrier resonant tunneling diodes.[5] Although these diodes are a short version of a superlattice structure, they still demonstrate the interactions between quantum wells. Our data reveal new features about energy level alignment. Our data show that a current peak is observed when any energy level in the two wells is resonant with the emitter level, without energy level alignment between neighboring wells. In addition, our data show that tunneling between next-to-nearest wells can be as strong as tunneling between nearest neighbors. One sample showed inverted bistability, where upward sweep shows lower current than downward sweep. We explain that the bistability is related to the X state in AlAs barrier.

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II. EXPERIMENTS

The structures used in this study are made of $In_{0.53}Ga_{0.47}As$ wells and AlAs barriers, grown by molecular beam epitaxy (MBE) on n^+ InP substrates. The triple barrier structure is made of (starting from the substrate side) AlAs barrier, narrow InGaAs well, AlAs barrier, wide InGaAs well, and AlAs barrier. Three different structures A, B, and C were grown. In these structures, the width of the narrow well was fixed to 58 Å. The widths of the wide well and the barrier are 71 and 25 Å, respectively, for sample A; 65 and 25 Å for sample B; 65 and 35 Å for sample C. The contacting layers on the top and the substrate side are Si doped InGaAs layers with 7×10^{17} cm^{-3} doping density. An undoped InGaAs spacer (64 Å) was inserted between the contacting layers and the triple barrier structure. An Au disk of 50 or 100 μm diam was deposited for an ohmic contact, which also serves as a mesa etch mask. Current–voltage characteristics were measured at room temperature and 77 K using a Hewlett–Packard 4142B dc source/monitor.

We calculated energy levels and wavefunctions of triple barrier resonant tunneling diode (RTD) structures. The energy levels and wavefunctions were obtained by matching wavefunctions [$\exp(\pm ikx)$, $\exp(\pm qx)$] and their derivatives at the six interfaces between InGaAs and AlAs. Nonparabolicity was included by using the method in Ref. 6.[6,7] Figure 1 shows squares of electron wavefunctions in sample B. The calculated wavefunctions are localized in a single well with only small penetration into the other well, due to the thick barriers. The four energy levels in Fig. 1 are equivalent to the first and second energy levels in the two wells, and we call these n_1 and n_2 for the levels in the narrow well, and w_1 and w_2 for those in the wide well. The calculated energies for sample B are $w_1=134$, $w_2=389$, $n_1=159$, and $n_2=435$ meV. For sample C (35-Å-thick barriers), the calculated energies are within ±2 meV of those in sample B.

Figures 2 and 3 show room temperature and 77 K I–V characteristics measured in the triple barrier diodes. At a positive bias, the top side is positively biased, and the substrate side becomes the emitter. Although the current scale is different for the three samples, the peak voltages are nearly the same, which are marked by the vertical lines. In the fig-

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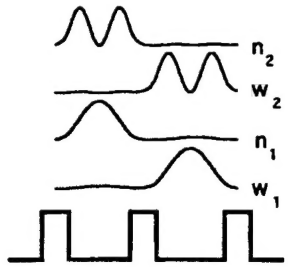

FIG. 1. Squares of electron wavefunctions calculated in sample B. Substrate is on the left side of the triple barrier diode structure.

ures, the peak positions are named by the energy levels. The relation between the peaks and the energy levels will be discussed later. Sample C has thicker barriers, so that the peak positions are slightly higher than those of sample B. (Samples A and B are different in the wide well width, and samples B and C are different in the barrier thickness). In Fig. 2, two current peaks are observed on the positive side (0.65 and 1.10 V), and two peaks on the negative side (−0.25 and −0.82 V). The peak at −0.82 V becomes stronger in the 77 K data shown in Fig. 3. In addition, Fig. 3 shows another peak at 0.32 V. This peak becomes clear in the dI/dV curve, and the position is marked as a dashed line in Fig. 2. In Fig. 3, sample B shows inverted bistability around 1.2 V.

In Fig. 4, we show I–V data for a larger bias range up to ±4 V. The upper curve is from a 50 μm diam device of sample B, and the two lower curves are from a 100 μm diam device of sample C. The solid curves were measured at room temperature, and the dashed curve was measured at 77 K. Note that four peaks are observed on the positive and negative sides of sample C. Sample B (50 μm device) also shows four peaks in the negative side. In sample B, the small peak positions (w_1 and n_1) are the same as those of sample C, but

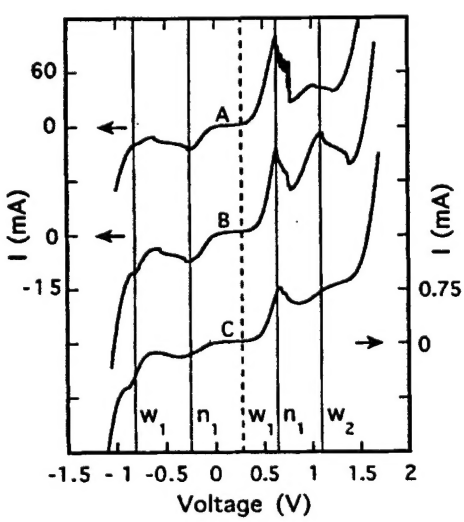

FIG. 2. I–V characteristics of 100 μm diam devices of samples A–C, measured at room temperature. The sequence of electron flow for positive bias is emitter—narrow well—wide well.

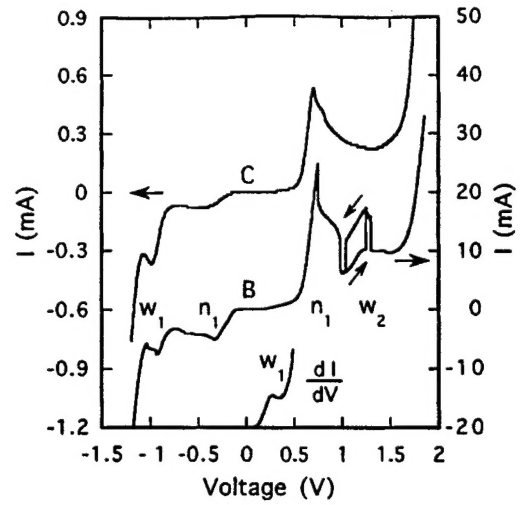

FIG. 3. I–V characteristics of samples B and C (100 μm diam) measured at 77 K, and derivative of sample B's I–V. In the I–V curve of sample B, the arrows around 1.2 V indicate voltage sweep direction.

the two large peak positions on the negative side (n_2 and w_2) are different from those of sample C. The n_2, w_2 peak positions of sample B were not the same when different pieces from the same wafer were measured, and we think that this variation is due to peak voltage shift from the large current.

III. DISCUSSIONS

It is important to note that four current peaks are observed in a two-well RTD structure, in which each well has two energy levels. Our structures have five energy levels: one is the emitter level, and the other four are the quantum well levels. If the quantum well energy levels have to align to make current peaks, a maximum of three peaks should be observed at both polarities of bias. The three peaks at negative bias would be $e-w_1-n_1$, $e-w_1-n_2$, and $e-w_2-n_2$, where e is the emitter level. The alignment $e-w_2-n_1$ is not allowed because the w_2 level is much higher than

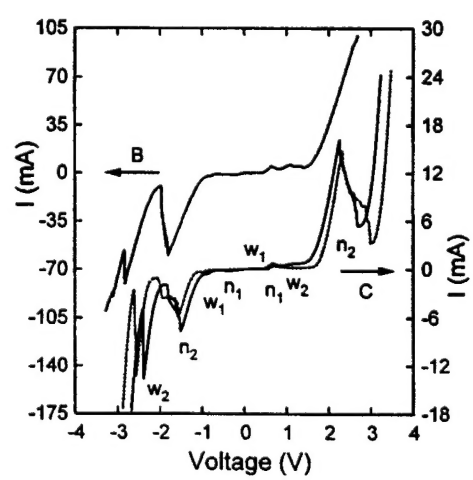

FIG. 4. I–V characteristics of 50 μm diam sample B and 100 μm diam sample C for a larger bias range. Solid curves were measured at room temperature, and dashed curve was measured at 77 K.

TABLE I. Energy levels obtained from the I–V peak positions of sample C, and calculated from the Schrödinger equation. Wide well width is 65 Å, and narrow well width is 58 Å. X state energy was obtained from w_2 peak of sample B.

Energy level	Positive bias	Negative bias	Calculation
w_1	0.22eV	0.33eV	134meV
w_2	0.72eV	0.89eV	389meV
n_1	0.25eV	0.24eV	159meV
n_2	0.80eV	0.98eV	435meV
X	0.54eV		

n_1 level. At a positive bias, the three peaks would be $e-n_1-w_1$, $e-n_1-w_2$, and $e-n_2-w_2$. In the level alignment picture, a total of six peaks should be observed, but our data show eight peaks. We believe that the peaks observed in our data are from resonant tunneling between the emitter level and one of the quantum well levels, not from the level alignment between neighboring wells.

Instead of using a level alignment picture, we can relate the four current peaks to the four individual energy levels in Fig. 1. In this picture, the current peaks show up when any quantum well level and the emitter level are resonant. On the positive side, the four peaks are w_1, n_1, w_2, and n_2 resonances. On the negative side, they are n_1, w_1, n_2, and w_2. This is shown in Figs. 2–4. We tried to calculate energy levels from the peak positions in the I–V data. In the calculation, we assumed that the Fermi level at the end of the spacer is in resonance with the quantum well energy level. Depletion was not included, since at high doping density it does not make much difference in peak voltage. The energy level of a double barrier RTD (55 Å InGaAs well, 25 Å AlAs barrier, 2×10^{18} cm^{-3} doping density) calculated by this method was 0.20 eV, which is half of the peak voltage. The results for triple barrier diodes are listed in Table I. They are much larger than those from the Schrödinger equation, but compared to 0.20 eV of the double barrier structure they are acceptable. The values on the negative bias are larger than those on the positive side, and this could be due to asymmetric dopant distribution. Although the energy levels obtained this way is larger than those from the calculations, the overall behavior supports that the current peaks in our data are from the four energy levels.

The w_2 peak (1.1 V) of sample B showed a thermally activated behavior. When the temperature was lowered, the peak current decreased, while other peaks remained almost unchanged. This means that around 1.1 V bias there is an energy level which is slightly higher than w_2 level. But the n_2 level is too high to be thermally activated, and we think that this is due to the X state in the middle AlAs barrier. By assuming that this is X assisted w_2 peak, we obtained 0.54 eV for the X state energy. The AlAs X state is located at 0.14 eV from GaAs conduction band edge, and the conduction band energy difference between $In_{0.53}Ga_{0.47}As$ and GaAs is estimated at about 0.4 eV, so that this is in good agreement with 0.54 eV obtained above.

In Fig. 3, sample B shows inverted bistability at 77 K in the region around 1.2 V. The bistability disappeared below 50 K when the peak current was small. The inverted bistability has been reported before in a double barrier structure,[8] and it was explained by charge build up in the well. In our picture, the peak at 1.27 V is due to the resonance between the emitter level and the second level (w_2) in the wide well, and assisted by the X state in the middle barrier. We think that the bistability is related to the charge build up in the AlAs barrier. In sample A, the wide well width is 71 Å, and the energy separation between w_2 level and the X state is larger, so that the bistability is not observed.

One of the strong peaks in the negative side (Fig. 4) is a resonance between the emitter and the narrow well (n_2). In this bias polarity, the emitter and the narrow well are not the nearest neighbors, since the wide well is in between them. It means that a resonance between next-to-nearest wells can be as strong as the resonances between the nearest wells. This kind of resonance in a superlattice has not been considered so far. In a superlattice, each well can be the emitter for the wells in the low energy side, and it was assumed that only the nearest neighbor can be a current source. In contrast, our data indicate that a well can inject electrons farther than to its nearest neighbor. This can be explained by considering the length of the localized electron wavefunctions in a superlattice.[9] If the wavefunction covers more than one period of a superlattice, it will be possible to observe this type of resonance.

There can be other mechanisms to explain the four peaks, such as phonon assisted tunneling. In I–V data, phonon assisted tunneling peak follows the main peak, and is very weak at room temperature.[10] From the characteristics of our peaks, we think that they are not originated from phonon assisted tunneling.

IV. CONCLUSION

We present transport data measured in triple barrier resonant tunneling diodes. Current peaks are observed when any energy level in the wells becomes resonant with the emitter level. Our data indicate that the energy levels in the neighboring wells are not aligned, and the resonance condition can also be satisfied between next-to-nearest neighboring wells. One of the peak showed thermally activated behavior and bistability. We explain that this is due to X assisted tunneling when the X state and one of the energy levels is energetically close.

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Effect of doping density on capacitance of resonant tunneling diodes

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We studied capacitance and parallel resistance in resonant tunneling diodes as a function of the doping density in the emitter and the collector regions. Capacitance was obtained by analyzing resonance in the admittance measured. Our data show that the capacitance varies with the doping density, and that the capacitance is smaller than the value expected from the growth parameters. Electron density modulation exists around the barriers, and capacitance has doping density dependence as a result of the modulation. © *1997 American Institute of Physics.*
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INTRODUCTION

In a resonant tunneling diode (RTD), capacitance is an important parameter in determining its high frequency characteristics. There have been reports about capacitance measurements in RTD structures,[1–3] but the effect of doping density in the emitter and the collector has not yet been analyzed. In this work we investigated the device parameters of a RTD as a function of the doping density. The RTD capacitance was usually obtained from the slope of the imaginary part of the admittance, which was measured by an impedance meter at a fixed frequency. This method, however, is not accurate because a RTD device is a combination of resistance, capacitance, and wire inductance.

In order to obtain an accurate capacitance value, we used resonance of the RTD. It was determined that the Au wire (18 μm diameter, 4 mm long) used in the RTD connection had about 8 nH of inductance. This is larger than the theoretically expected value of 3 nH,[4] because of the magnetic material used in the header where the RTD is mounted. When a RTD is connected by the Au wire, the whole circuit becomes a series inductance-capacitance (LC) circuit due to the wire inductance and the RTD capacitance, and a LC resonance is observed in the admittance. For a 100 μm diameter RTD, the resonance frequency is in the range of 300 MHz–500 MHz, depending on the RTD capacitance. We measured the admittance by sweeping the frequency up to 1 GHz, using a Hewlett-Packard 4191A RF impedance analyzer. The RTD capacitance and the parallel resistance were obtained by fitting the calculated admittance to the measured data. The admittance changed drastically around the LC resonance frequency, and the device parameters could be easily extracted because the resonance behavior was very sensitive to the parameter changes.

EXPERIMENTS

The structures used in this study were made of $In_{0.53}Ga_{0.47}As$ layers grown by molecular beam epitaxy (MBE) on n+ InP substrates. Four samples (A, B, C, and D) were investigated. The double barrier structure is composed of an InGaAs well with AlAs barriers attached on both sides of the well, all undoped. The growth parameters of the four samples are listed in Table I. In all samples the well width was fixed at 51 Å. The R, L, and C values in Table I were obtained from the admittance data, the details of which will be discussed later. The contacting layers outside the double barrier structure are 1000 Å thick Si-doped InGaAs, with the doping density N_D ranging from 8.6×10^{15} cm^{-3} to 2.0×10^{18} cm^{-3}. An undoped InGaAs spacer layer was inserted between the contacting layer and the double barrier structure. A 100 μm diameter Au disk was deposited as an ohmic contact, and also served as a mesa etch mask. An 18 μm diameter Au wire of 3–5 mm length was bonded to the Au disk for the connection.

Figure 1 shows the current-voltage characteristics of samples A and C, measured at room temperature. The data were measured by a Hewlett-Packard 4142B dc source/monitor. Since sample C has a lower doping density, its peak voltage is higher than that of sample A. The lower peak current of sample A is due to the thicker barriers. Current oscillations were observed in sample C when it was biased in the negative differential resistance region.

The admittance (Y) of sample A measured by the RF impedance analyzer is shown in Fig. 2. Figure 2(a) is without any bias voltage, and Fig. 2(b) is with 0.45 V bias applied. The dots in Fig. 2 represent experimental data, and the solid curves represent calculated results using the circuit model of the Fig. 2. The real part (Y_0) shows a sharp peak at the resonance frequency, while the imaginary part (Y_{90}) changes from a positive to a negative value as the frequency (f) is increased beyond the resonance frequency. To clarify the origin of the inductance in our device, we compared the inductances of the wire connected between the terminals of the header, one with a RTD mounted to it, and one without a RTD. The two inductances measured this way were nearly equal for the same wire lengths. In addition, the measured inductances were proportional to the wire length. Thus it is obvious that the inductance in the RTD system originates from the Au wire.

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TABLE I. Growth parameters and measured R, L, C values for the four samples.

	A	B	C	D
AlAs barrier (Å)	32	25	25	25
InGaAs spacer (Å)	64	64	64	16
Doping density N_D (10^{16} cm)	2.0	2.0	0.86	46
R_{EXT} (Ω)	1.8	1.9	2.4	9.9
L_{EXT} (nH)	8.3	7.0	8.3	8.9
R_D (Ω)	1250	350	260	630
C_D (pF)	16.5	17.8	15.8	30.3

EQUIVALENT CIRCUITS OF THE RTD

We modeled the RTD as a parallel circuit of C_D and R_D, with an external inductor and resistor (L_{EXT}, R_{EXT}) connected in series to the RTD. This model is shown in Fig. 2(a). The R, L, C values listed in Table I were obtained by fitting the calculated frequency characteristics to the $f-Y$ resonance data, measured at zero bias voltage.

When a bias voltage is applied to a RTD, the thermionic current increases, and the parallel resistance R_D decreases. The height of the Y_0 peak is reduced by the applied bias as shown in Fig. 2(b), since any decrease in R_D lowers the Q factor of the resonance circuit. Figure 2(a) shows the admittance of sample A at zero bias voltage. In Fig. 2(a), the slope of Y_{90} in the low frequency region is 16.5 pF, which is the same as the value obtained from the resonance fitting. In Fig. 2(b), the Y_{90} slope is decreased by the applied bias, but the slope is different from the capacitance obtained by the fitting. (The slope of Y_{90} is 7.2 pF, while the capacitance from the fitting is 11.3 pF.) We calculated the admittance of the circuit in Fig. 2 for different R_D and L_{EXT} values to see their effect on the Y_{90} slope.

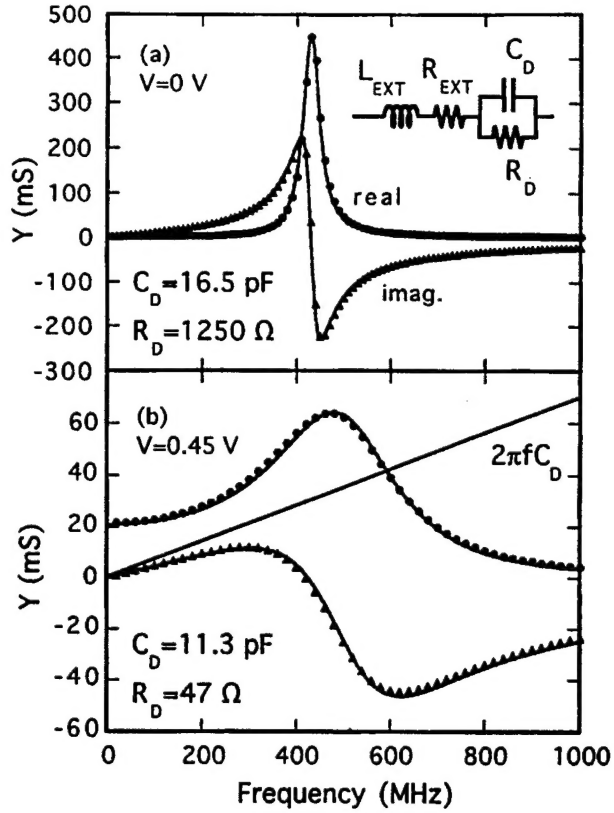

FIG. 2. Frequency dependent admittance of sample A at (a) 0 V and (b) 0.45 V bias voltage. The solid curves are calculated results, and the dots are measured data. The straight line in (b) is for C_D= 11.3 pF.

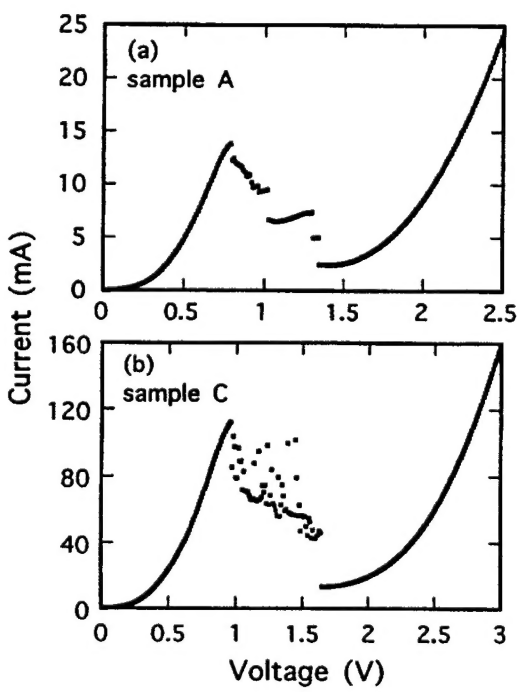

FIG. 1. Current-voltage characteristics of samples A and C measured at room temperature.

Our calculations show that when R_D is small, the slope of Y_{90} is lower than C_D. In addition, for R_D<60 Ω [other parameters being fixed to those values in Fig. 2(b)], the presence of L_{EXT} also lowers the slope of Y_{90}. This means that the slope of Y_{90} gives lower capacitance values when either L_{EXT} or R_D exists in the circuit. Since a RTD is made of R and C, and is connected by an Au wire which has non-negligible inductance, only frequency sweeping as shown in Fig. 2 can give correct C_D values.

In Fig. 3 we show C_D (circles) and R_D (triangles) measured in sample A, as a function of applied bias. The solid line represents calculated capacitance using the depletion model in Ref. 2, with an initial separation of 590 Å. Although there is a discrepancy between the data and the calculation, the measured and calculated capacitances behave in similar ways. Due to the internal resistance of the impedance analyzer, the sample could not be biased in the negative differential resistance (NDR) region (0.8 V–1.3 V), where a capacitance peak was observed before.[2] R_D would have large negative and positive peaks in the NDR region, and the larger R_D shown at the higher bias is a decreasing part of the resistance peak. In Fig. 3 R_{EXT} obtained from the fitting increased with applied bias, from 1.8 Ω to 4.0 Ω. We think that this increase is due to the series resistance in the depletion region of the collector. At a higher bias L_{EXT} decreased

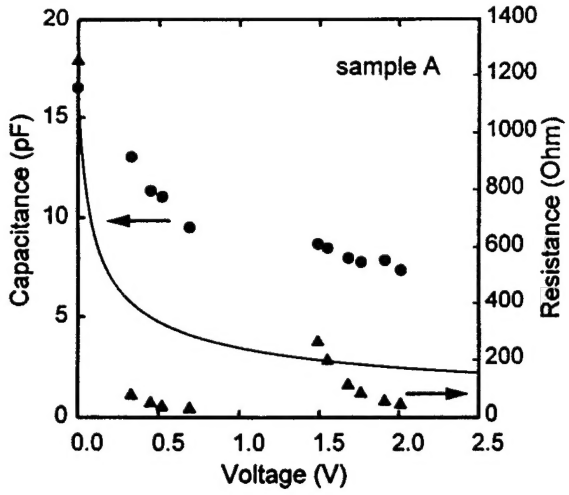

FIG. 3. Capacitance and parallel resistance of sample A as a function of bias voltage. The circles represent capacitance, and the triangles represent parallel resistance. The solid line was calculated from the depletion model.

from 8.3 nH to 7.4 nH. An inductance change by applied bias was recently reported in Ref. 3, and it was suggested that the current delay time change in the quantum well was the reason for the change. In our structures the inductance from the Au wire is much larger, and at this point we do not understand the reason for the inductance decrease.

DISCUSSION

In Fig. 4 we plotted zero voltage capacitance as a function of the doping density. The data labelled U in the figure is from Ref. 3. The inverse of the capacitance is shown by circles, and the emitter-collector distance from the growth parameters is shown by triangles. Here, the inverse of the capacitance is $A\epsilon/C_D$, where A is the area of a RTD, and ϵ is the dielectric constant (14 ϵ_o for InGaAs). It was expected

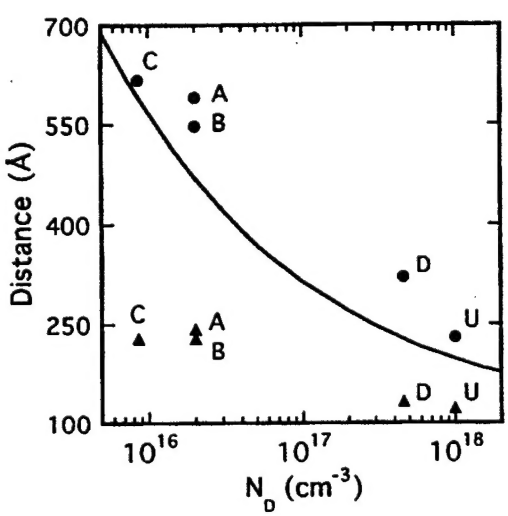

FIG. 4. The inverse of the measured capacitance (circles) and the emitter-collector distance (triangles) from the growth parameters. The solid line is the calculated distance between the emitter and the collector. The data labelled as U are from Ref. 3.

that the inverse of the capacitance at zero bias voltage would directly reflect the emitter-collector distance, independent of the doping density N_D in the emitter. However, Fig. 4 shows that C_D depends on N_D, and the inverse of the capacitance is much longer than the growth parameter. When $N_D=2.0\times10^{16}$ cm^{-3}, the C_D's of a 100 μm diameter RTD are 16.5 pF (sample A) and 15.8 pF (sample B), while the C_D of 4.6×10^{17} cm^{-3} (sample D) is 30.3 pF under the same conditions. The inverse of the capacitance is 590 Å for 16.5 pF and 321 Å for 30.3 pF. In comparison, the distances between the emitter and the collector from the growth parameters (including spacer layer) are 243 Å for sample A and 133 Å for sample D.

We discuss the doping dependence of the capacitance by considering the shape of the wave functions in the emitter and the collector. The wave functions in the emitter and in the collector can be expressed as $\psi(z)\exp(ik_Xx+ik_Yy)$, where z is along the growth direction. Without a barrier, $\psi(z)$ will be $\exp(ik_Zz)$. When a barrier is introduced at $z=0$, $\psi(z)$ changes to $\exp(ik_Zz)+R\exp(-ik_Zz)$ for the $z<0$ region, where R is the reflection coefficient. If the barrier is high, there is full reflection ($R=-1$, $\psi(z)\propto\sin(k_Zz)$), and the electron density has a sine wave shape starting from zero at the barrier interface. In the RTD case, the AlAs barrier height is 1 eV, and the electron energy is around 100 meV, so we can expect large reflection and electron density modulation near the barriers. Because of the charge modulation, the distance between the electron systems in the emitter and the collector is larger than the growth parameter. Since the doping density N_D determines the Fermi energy level in the doped region, capacitance will have doping density dependence. When N_D increases, higher k_Z states are occupied, and electron density will reach N_D in a shorter distance.

When an electron profile has a shape distributed over a finite width, the capacitance should be calculated by considering the change in the electron profile due to the applied voltage.[5] For a RTD structure we can approximate the distance between the points where electron density reaches N_D to be the emitter-collector distance. The capacitance in a two-dimensional electron system was calculated in a similar way with a numerical constant multiplied.[5]

We plotted the distance calculated for sample A as a function of N_D (solid line) in Fig. 4. The electron density was calculated by solving the Schrödinger equation numerically. Although there is about a 100 Å discrepancy, the calculated distance shows similar doping density dependence as the inverse of the capacitance (circles). It is evident that the distance from the growth parameters (triangles) is too small to explain the measured capacitances. We believe that the general agreement between the data and the calculation demonstrates that RTD capacitance is determined by the charge modulation in the region around the barriers.

We reported previously that a capacitance peak was observed in the NDR region,[2] where the peak was explained by a charge buildup in the quantum well. The charge buildup in the well makes the emitter-collector distance shorter, and the capacitance shows a peak structure. In our previous work the

admittance was measured at a single frequency, and the slope was taken as the capacitance. As mentioned in the beginning, this method gives lower capacitance values, and the actual capacitance value is larger than the values shown in Ref. 2. Therefore, our observation that the measured capacitance was much larger than the depletion capacitance is still valid.

The doping density dependence can be explained by an electrostatic model, where electrons spill into the undoped region in a *n-i-n* structure.[6] However, in a small dimension structure, the exact nature of charge distribution near the barriers should be described by the Schrödinger equation, and the electrostatic model can give wrong answers.

When N_D was increased to 2×10^{18} cm^{-3}, R_D at zero bias voltage dropped to 5 Ω, and the LC resonance behavior disappeared (not shown here). LC resonance also disappeared at high bias when R_D became small. It is believed that the small R_D shorted the capacitance to change the whole system into a L-R circuit.

In our calculations the electron density in the quantum well increases with N_D. This electron density is a tail of the wave functions in the emitter and the collector. The electron density in the well increases with N_D, since higher k_Z is occupied at higher N_D. We can roughly estimate the order of magnitude of the electron density to be $N_D|\psi_O/\psi_P|^2$. Here, ψ_O is ψ at the center of the well, and ψ_P is the peak value in the doped region. In our calculations $|\psi_O/\psi_P|^2$ changed by a large amount when N_D changed. The ratio $|\psi_O/\psi_P|^2$ at $N_D=2\times10^{18}$ cm^{-3} is about 0.006, and the electron density in the well could be as high as 10^{16} cm^{-3}. At this high density we can expect strong conduction between the emitter and the collector. This is in agreement with the observation of low R_D (5 Ω) at $N_D=2\times10^{18}$ cm^{-3}.

CONCLUSIONS

We obtained the capacitance and parallel resistance of resonant tunneling diodes by measuring frequency dependent admittance around a LC resonance frequency. The measured capacitance showed doping density dependence. We explained that electrons in the emitter and the collector were separated from the barriers by a finite distance, since the wave functions were a sine wave shape starting from the barrier. Our calculations explained the behavior of C_D and R_D at different N_D's. The information obtained by this method will be important in designing a RTD with improved high frequency performance.

ACKNOWLEDGMENTS

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Observation of Resonances by Individual Energy Levels in InGaAs/AlAs Triple-Barrier Resonant Tunneling Diodes

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Current-voltage characteristics in InGaAs/AlAs triple-barrier resonant tunneling diodes were investigated. Our data show that a current peak is observed when any of the quantum well energy levels is resonant with the emitter level, without level alignment between neighboring wells. When one of the well widths was increased, some peak voltages shifted, while others remained unchanged. This indicates that the peak positions are associated to a specific well. When the temperature was lowered, some peaks became stronger, while others became weaker. Our analysis shows that the weaker peaks are caused by the resonances between the emitter and the far side well. At low temperatures, current injection to the far side well is more difficult, and the current peak becomes weaker. These results indicate the conculsion that neighboring energy levels are not aligned in these structures.

KEYWORDS: level alignment, resonant tunneling, charge build-up, temperature dependent current, electric field distribution, triple-barrier diode

1. Introduction

Electric field distribution in a superlattice structure is important for determining the performance of vertical transport devices. At low-bias voltage, the electric field is uniformly distributed within the structure. At higher voltages, the electric field is no longer uniform because a high field domain is formed.[1)] It was previously thought that the electric field in a superlattice always aligns the energy levels of the neighboring wells at the same height. Recently, there was an experimental report that the electric field in a superlattice is lower than the field for resonant alignment.[2)] The report showed that resonant alignment of energy levels occurred only for a narrow region of bias. In order to investigate electric field distribution, we studied the current-voltage (*I-V*) characteristics of triple-barrier resonant tunneling diodes.[3)] Although this structure has only two wells, it demonstrates the interactions between quantum wells. Our data show that a current peak is observed when any energy level in the two wells is resonant with the emitter level, but shows no energy level alignment between neighboring wells. Peak voltage shift could be related to the well width change, and current peaks showed two different types of temperature dependence. These results indicate the conculsion that energy levels in neighboring wells are not aligned.

2. Experiments

The structures used in this study are made of $In_{0.53}Ga_{0.47}As$ wells and AlAs barriers, grown by MBE on n^+ InP substrates. The triple barrier structure consists of (starting from the substrate side) an AlAs barrier, narrow InGaAs well, AlAs barrier, wide InGaAs well, and AlAs barrier. Three different structures; A, B and C were studied. In these structures, the width of the narrow well is fixed to 58 Å. The wide-well width is 71 Å for sample A, and 65 Å for samples B and C. The barrier thickness is 25 Å for A and B, and 35 Å for C. The contacting layers on the top and the substrate side are InGaAs layers with $7 \times 10^{17}\,cm^{-3}$ Si doping density. An Au disk of 100-μm diameter was deposited for an ohmic contact. Current-voltage characteristics were measured using a Hewlett-Packard 4142B dc source-monitor.

We calculated the energy levels and wavefunctions by numerically solving the Schrödinger equation. The calculation results show two energy levels in each well, and the calculated energies for sample B are 134 and 389 meV for the wide well, and 159 and 435 meV for the narrow well.

Figure 1 shows the *I-V* characteristics measured at room temperature. At positive bias the top side is positively biased, and electrons flow from the substrate through the narrow and wide wells. In this figure, the peak voltages are similar for the three samples, although the current scale is very different. At low temperature, one more current peak was resolved at 0.3 V (shown in Fig. 4 inset), and the position is indicated by a dashed line in Fig. 1. Sample C has thicker barriers, so that the peak positions are slightly higher than those of sample B. Figure 2 shows the *I-V* data of sample C taken

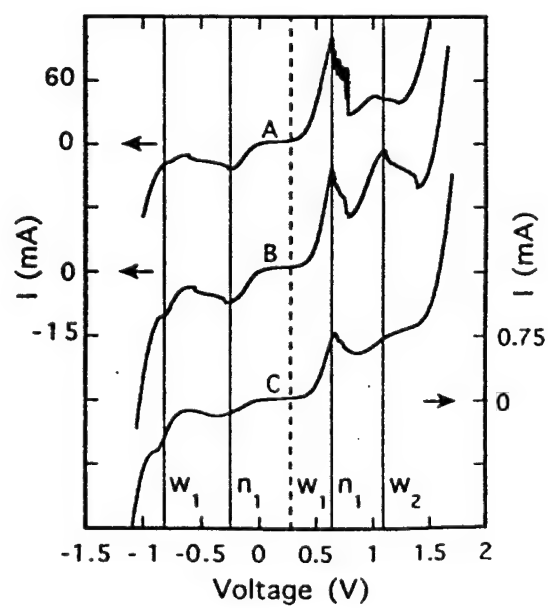

Fig. 1. Current-voltage characteristics of the three samples measured at room temperature.

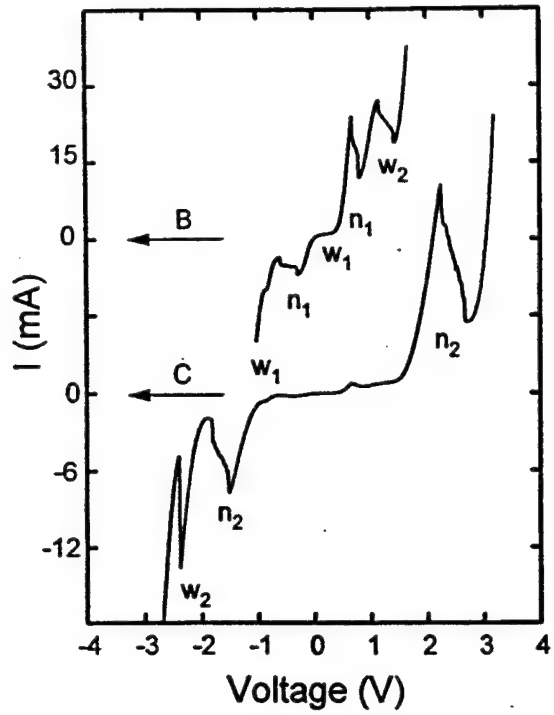

Fig. 2. Current-voltage data for a larger bias range, measured at room temperature.

at higher bias range. Samples A and B did not exhibit any peaks in the higher voltage region. In this figure, four peaks are observed in one polarity of bias for sample C. If the levels were aligned, the maximum number of peaks would be three. Therefore, we can infer that the four peaks in our data are from the resonances of the four energy levels with the emitter level, and the peaks in the figure are named by the associated energy levels. They are n_1, w_1, n_2 and w_2 on the negative side, and w_1, n_1, w_2 and n_2 on the positive side.

Figure 3 shows how the peak positions respond to well-width change. In this figure, the *I-V* data of samples A and B are compared. Samples A and B are different only in wide-well width. The width of the wide well is 71 Å for sample A and 65 Å for sample B. In Fig. 3(a) the n_1 position is nearly fixed, but the w_2 position shifted to lower voltage when the wide-well width was increased in sample A. Figure 3(b) shows negative-side peak positions. In this figure the w_1 peak also shifted to lower voltage in sample A. The Fig. 3(c) 77 K *I-V* data clearly show that the w_1 peak position is shifted to lower voltage. Figure 3(c) also shows that the two peaks on the negative side (sample A) are merged into one peak with one wide negative differential resistance region. The shift of the peaks in sample A indicates that they are related to the wide-well width change. When the wide-well width was increased, the energy levels of the wide well were lowered, and the peak voltages were shifted to lower values. If the neighboring well levels are aligned, the change of well width in one of the wells should affect all of the peak positions. Our data show that the level alignment does not occur in this case.

In Figs. 4 and 5 we show the temperature dependence of *I-V* data. In Fig. 4, the w_2 peak at 1.2 V became weaker at low temperature, while the n_1 peak at 0.7 V became stronger. On the negative side, n_1 became weaker, while w_1 became stronger. Similar behavior is observed in the *I-V* data of sample C shown in Fig. 5. We believe that these results also support our individual resonance model. If current peaks show up as a result of individual level resonance, the peaks can be divided into two groups. One group contains the resonances between the emitter and the near side well, and the other group contains the resonances between the emitter and the far side well. For positive bias, the wide well is the far side well in our structures, and in Figs. 4 and 5 we can see that the w_2 peak is weaker at low temperature.

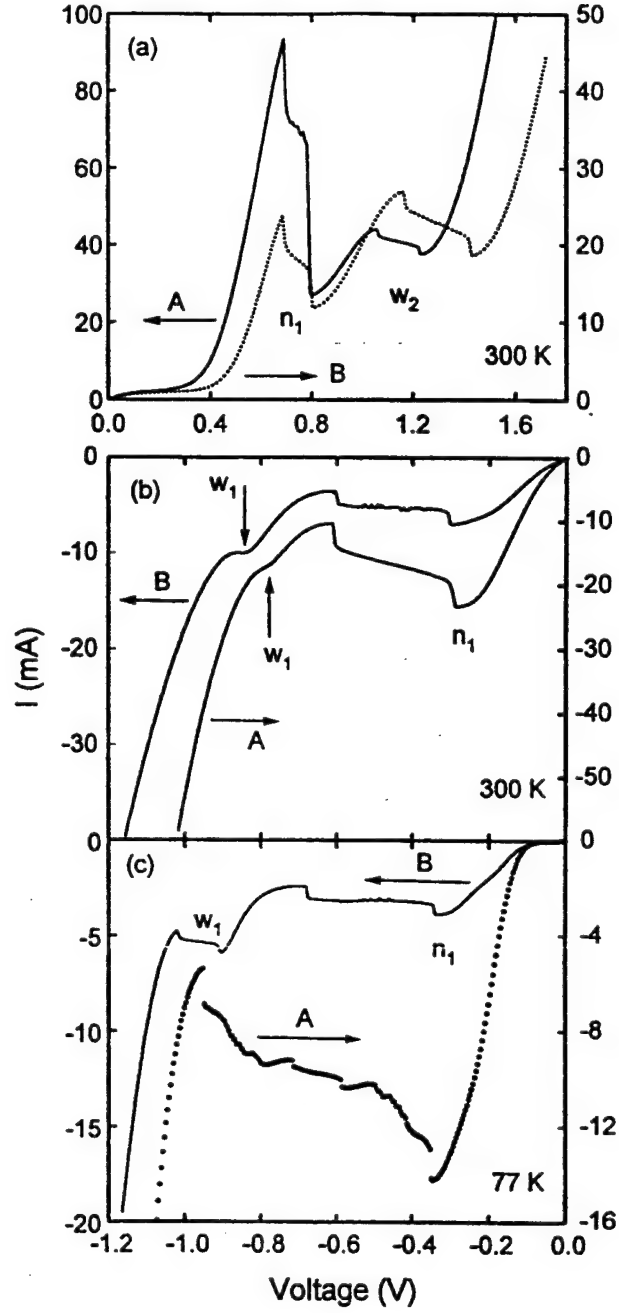

Fig. 3. Comparison of peak positions for samples A and B. (a) is for positive bias and (b) and (c) are for negative bias. The wide-well resonances (w_1 and w_2) clearly show shift when the width was increased from 65 Å to 71 Å.

When the structure is at the far resonance, the first well can be considered to be a barrier to the far side well. The transmission through the first well can be altered by temperature, since the transmission depends on the energy level position and thermal activation. The energy levels in the first well are

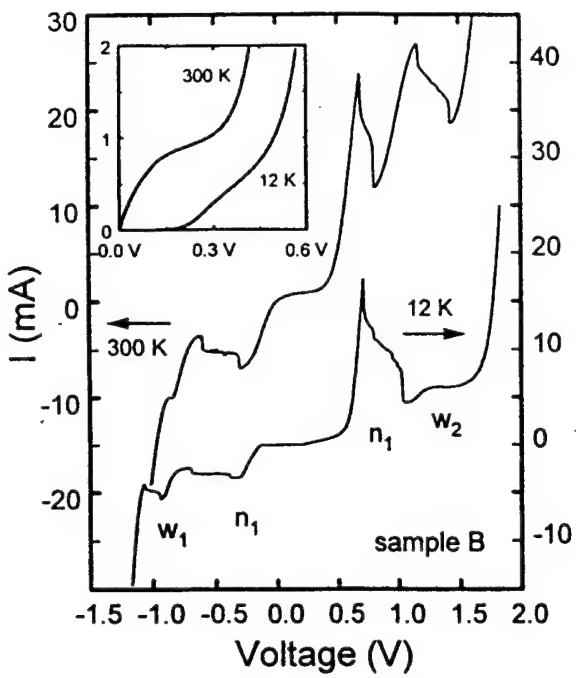

Fig. 4. Temperature dependence of the resonances in sample B. n_1 on the negative side and w_2 on the positive side became weaker at low temperatures. Inset: *I-V* characteristics of sample B on an expanded scale, between 0 and 0.6 V.

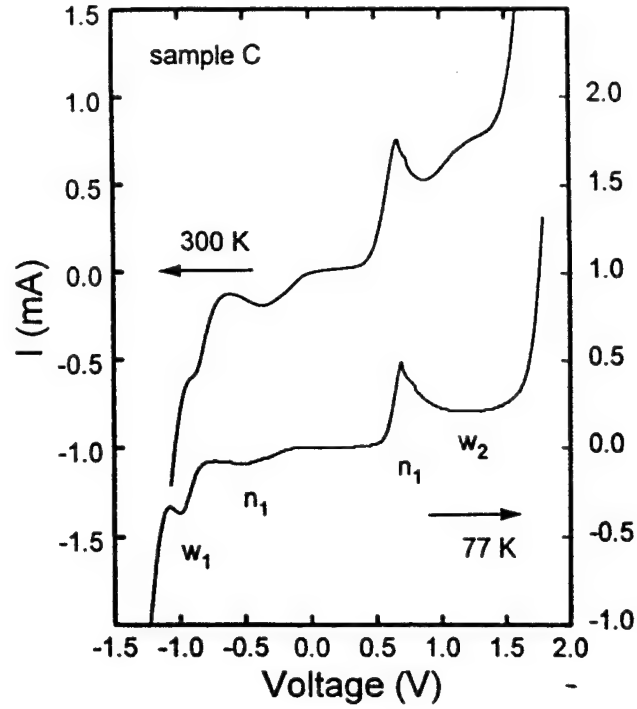

Fig. 5. Temperature dependence in sample C. The behavior is similar to those in Fig. 4.

not resonant to the emitter, and at room temperature, current can flow via thermal excitation. At low temperature, thermal activation becomes difficult, and transmission through the first well decreases. In other words, the effective barrier becomes thicker at low temperature. This explains why the far resonance shows weaker resonance at low temperature.

3. Conclusion

We presented experimental evidence which supports our individual resonance model. The number of peaks, well-width dependence and temperature dependence indicate that the peaks in our data are due to resonances between the emitter and independent energy levels, without level alignment between neighboring wells.

We would like to note that this model does not deny the occurrence of charge accumulation in quantum wells. Charge accumulation in the wells could exist, but apparently the charge accumulation is not strong enough to align neighboring energy levels to the same height. In some of our low temperature *I-V* data we observed bistability, which we think is due to charge accumulation.

We demonstrated with our data that the resonance between wells with one well in between can show peaks, especially at room temperature. So far. only resonances between adjoining neighbors were considered in a superlattice structure. However, our data show that a well can inject electrons farther than to its joining neighbor. This can be explained by considering the length of the localized electron wavefunctions in a superlattice.[4] If the wavefunction covers more than one period of a superlattice, it will be possible to observe this type of resonance.

In Fig. 3(c), two peaks were merged into one wide peak at 77 K (sample A). This behavior has not been previously reported. In a multi-barrier structure, it was not clear whether two closely spaced levels merge into one peak or remain separated by anti-crossing. Our data show that merging can occur in such a case.

Acknowledgements

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A New Submillimeter Wave Semiconductor Source--Bipolar Injection Transit Time Diode (BIPOLITT)

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Abstract

We have proposed and analyzed a new submillimeter and deep millimeter wave transit time device named BIPOLITT (Bipolar Injection and Transit Time). The device structure is similar to a Heterojunction Bipolar Transistor (HBT) with the base terminal open circuited to AC signal. The ambipolar diffusion process in the relatively long base is used to achieve a phase delay of the injection current close to $180°$ (relative to the total current). The collector depletion region is used as the drift zone. As an example, a BIPOLITT diode for 300-400 GHz is designed and analyzed. The small signal specific negative resistance is calculated to be about $-3\times10^{-7}\Omega cm^2$. A detailed large signal calculation at 300 GHz has shown an efficiency of at least 12% with about 2 mW output power without spurious oscillation. The BIPOLITT is expected to work up to at 1 THz.

Semiconductor device oscillators in the submillimeter and deep millimeter wave frequencies are recently being pursued by using Resonant Tunneling Diode (RTD) [1,2]. Currently, RTD sets the record of the highest oscillation at 712 GHz for semiconductor devices. In comparison, the highest frequency transistor oscillator to date is 213 GHz.[3] However, the power of RTD is very low, usually in the μW range [1,2]. The recent result of a 16 element RTD oscillator arrays designed with Schottky collectors and special bias circuits has reported 28 μW at 290 GHz [2]. The spurious oscillation [4,5] due to the inherent dc negative resistance of the RTD is the major difficulty in effectively applying the device, despite clever remedies proposed [5].

In this letter, we report for the first time the simulation results of a proposed new transit time device [6,7] called BIPOLITT (Bipolar Injection and Transit Time) for applications in submillimeter and deep millimeter frequencies. It uses a bipolar injection into the drift zone in a structure like HBT to generate RF powers. Detailed simulations in submillimeter and deep millimeter wave frequencies show good negative resistance and decent efficiency comparable to RTD but without the problem of spurious oscillation.

The transit time effects of the bipolar junction transistor (BJT) have been known in the early development of BJTs [8]. The effect has recently been analyzed in much more detail for applications using modern HBTs [9]. Even though negative resistance is expected, its has not been clearly demonstrated in experiment. One severe difficulty of applying the transit time effects in transistors at high frequencies is the detrimental RF signal loss which must come in through the base terminal. The other thing hindering the effective use of the transit time effects in transistors so far is the limited optimization of

the effects, i.e., only collector transit time is optimized [8,9]. We approach the problem from the point of view of a two terminal device and show for the first time: (1) the complete circumvention of the RF signal loss through the base by letting the base terminal RF open; (2) the importance of optimizing the base transit time to drastically enhance performance.

The basic structure of the proposed BIPOLITT is illustrated in Fig. 1(a). Electrons are injected from the emitter-base junction into the base. The neutral base region will provide a phase delay by the diffusion process. The delayed electrons are then injected into the collector depletion region which acts as the drift zone for producing the transit time negative resistance. The HBT technology allows the base doping to become higher than $10^{19} cm^{-3}$ [10] with a conductivity therefore larger than $10^{2} \Omega^{-1} cm^{-1}$ [7]. With this high conductivity, the dielectric relaxation time [7] is less than 10 femtosecond and the displacement current is less than 10% of the conduction current up to 1 THz. This means the charge neutrality implicitly assumed in the ambipolar diffusion equation [7,11] in the base is valid up to 1 THz.

In order to fully utilize the transit time, the injected current needs to have a phase delay (relative to the total current) close to $180°$ but still with a significant magnitude [6,7]. Is this feasible by the diffusion process in base? A quick way to the answer can be obtained by investigating the complete AC base transport factor α_T^*,which is the ratio of electron diffusion current at the end of the neutral base region to that at the beginning. It is well known that [11]

$$\alpha_T^* = \sec h[\frac{W_b}{L_{nb}}(1 + j\omega\tau_{nb})^{1/2}] \cong \sec h(j2.43\omega / \omega_b)^{1/2} \equiv \sec h(\Gamma), \quad (1)$$

where W_b is the thickness of the neutral base, $L_{nb} = \sqrt{D_{nb}\tau_{nb}}$ is the dc diffusion length, ω is the angular frequency, $\omega_b = 2.43D_{nb} / W_b^2$ is the base-cutoff angular frequency, τ_{nb} is the base minority carrier life time, and we define $\Gamma \equiv \sqrt{j2.43\omega / \omega_b}$. Since we are interested in the deep millimeter and submillimeter wave frequencies, $\omega\tau_{nb} >> 1$ and the term 1 in Eq.(1) can be neglected. At the base-cutoff ω_b, it is known that the magnitude of the α_T^* is reduced to about 71% with a corresponding phase delay of 58° [11]. To obtain a phase delay of 180° for α_T^*, it simply requires $\Gamma = \pi + j\pi$. The requirement demands $\omega \cong 8.6\omega_b$ and $|\alpha_T^*| = 0.09$. Then the collector injection current have a phase delay of 180° and a magnitude of 9 % relative to the conduction current at the emitter base junction. The base thickness should be designed to have a base cutoff frequency of 12% of the operating frequency. Therefore, it is possible to achieve a good injection phase delay to generate RF power with an efficiency of order of 10 % , which is very good at deep millimeter and submillimeter wave frequencies.

The accurate account of injection current phase delay should refer to the total current of the device. The ratio γ of the injection current with respect to the total current can be shown as

$$\gamma \cong \frac{(1/r_e)\Gamma \csc h(\Gamma)}{(1/r_e)\Gamma \coth(\Gamma) + j\omega C_{be}} \quad , \qquad (2)$$

where the emitter junction dc resistance $r_e = kT / qI_E$, with I_E as the dc emitter current. The C_{be} is the emitter junction depletion capacitance. The emitter efficiency is counted as one in Eq.(2) since a heterojunction at the emitter junction is used.

The numerator in Eq.(2) is the trans-admittance of the conduction current at the beginning of the collector drift region. We call it a trans-admittance because the voltage is referenced to the emitter-base junction. The denominator in Eq.(2) is the total admittance of the emitter-base junction. The equivalent circuit for the emitter junction can be constructed accordingly. Note that Eq.(2) is reduced to Eq.(1) if the displacement admittance $j\omega C_{be}$ is negligible when compared with the admittance $(1/r_e)\Gamma\coth(\Gamma)$ of the emitter junction conduction current. This is usually the case. Therefore, the earlier discussion of the ω dependence of α_T^* provides a general and simple trend for γ as well.

The equivalent circuit elements for the emitter-base junction have therefore three parallel elements: depletion capacitance, AC junction conductance and AC diffusion capacitance. The exact equivalent circuit in the base region is very complicated due to the ambipolar diffusion process. However, since the base doping is sufficiently high, it is a very good approximation to represent it by the base resistance parallel with the trans-admittance.

The equivalent circuit element for the collector depletion region is the well known transit time impedance Z_d of the drift region. It is determined [6,7] by the injection ratio γ and transit angle $\theta_d = \omega W_d / v_s$,

$$Z_d = \frac{1}{j\omega C_d}[1 - \frac{\gamma(1-e^{-j\theta_d})}{j\theta_d}], \tag{3}$$

where $C_d = \varepsilon_s / W_d$ is the specific capacitance of the drift region, with W_d and v_s the corresponding length and the saturation velocity therein. Both diffusion and velocity overshoot are neglected in Eq.(3). We have carried out more detailed simulations including both effects. Since Eq.(3) is obtained by an integration of the carriers in the drift region [6,7], we find the neglect of the diffusion is not serious for negative resistance. But we find as expected the diffusion effects are important for the accurate calculation of efficiency. The velocity overshoot effects is found to be negligible as long as the electric field in the drift region is sufficiently high.

The resultant small signal equivalent circuit including both the injector and the drift zone of the BIPOLITT is shown in Fig.1(b). We have accordingly designed a BIPOLITT for 300 to 400 GHz operation and have carried out extensive small-signal and large signal simulations. The details will be published elsewhere. In the following, we summarize our design and simulation results. The thickness of the base region (GaAs doped to $10^{19} cm^{-3}$) is designed to be $0.155 \mu m$, corresponding to a base-cutoff frequency of 65 GHz. The injection phase delay is about $170°$ at 400GHz and about $150°$ at 300 GHz. They are slightly larger than $180°$ to take advantage of a larger magnitude for γ. The thickness of the collector region (doped to $10^{17} cm^{-3}$) is $0.14 \mu m$ corresponding to a transit angle of about $180°$ at 400 GHz. The calculated specific resistance of the device shows a very broad negative resistance from 250 to 450 GHz. Compared to RTD, this negative resistance band is sufficient to circumvent the spurious oscillation problem. At 300 GHz with a bias current of $10^5 A / cm^2$, the specific resistance of the collector is $-5 \times 10^{-7} \Omega \cdot cm^2$. The specific resistance of the base is $1.3 \times 10^{-7} \Omega \cdot cm^2$. The specific

contact resistance can now be made smaller than $10^{-7}\Omega \cdot cm^2$ [10]. With an emitter (AlGaAs) doped to $10^{19} cm^{-3}$ with a thickness of $0.05\mu m$, the total specific resistance of the device is $-3\times10^{-7}\Omega \cdot cm^2$ at 300 GHz, comparable to that of RTD [13].

From the large signal simulation, we find the efficiency is at least 12% at 300 GHz. This efficiency is also comparable to that of RTD and much better than IMPATT. The corresponding efficiency of the HBT structure designed in [9] is found to be 3%. (This low efficiency is due to a phase delay too small in the base, less than 40°.) Our device can be biased by a current source through the emitter. When matched to a load of 3 Ω, an emitter area of about 10 μm^2 can be used. A resistor of about 10 $k\Omega$ across the base collector terminal will provide a DC bias voltage of 3 volt if the common emitter current gain β is about 40. This bias resistor is effectively an open circuit for the AC signal. Therefore, the foregoing two terminal analysis is valid and accurate. The maximum total output power of a single device is about 2mW at 300 GHz, limited by the breakdown voltage and the carrier space charge effects in the collector. Further calculations show that BIPOLITT can work up to 1 THz with an efficiency of about 5%. We have not optimized the performance by choosing other material systems and have not explored the effects of a drift field in the base region. The BIPOLITT can also be integrated in series without the dc instability problem of RTD [14].

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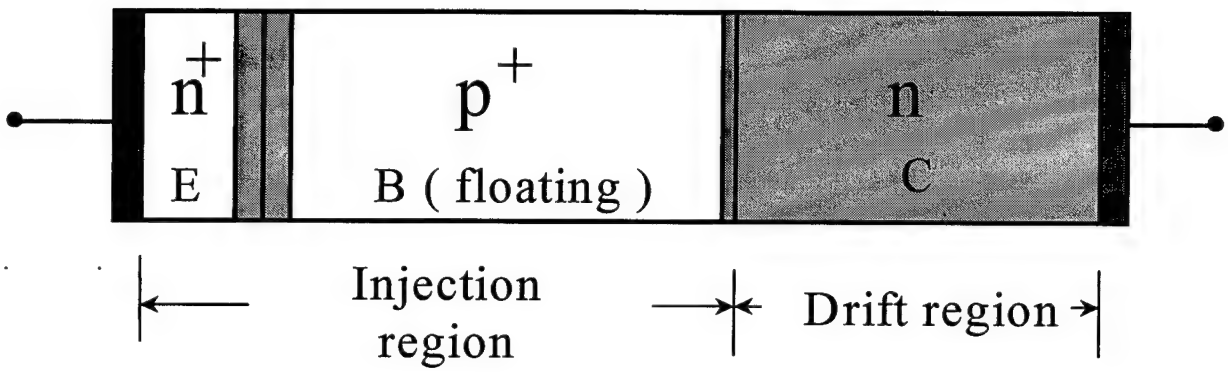
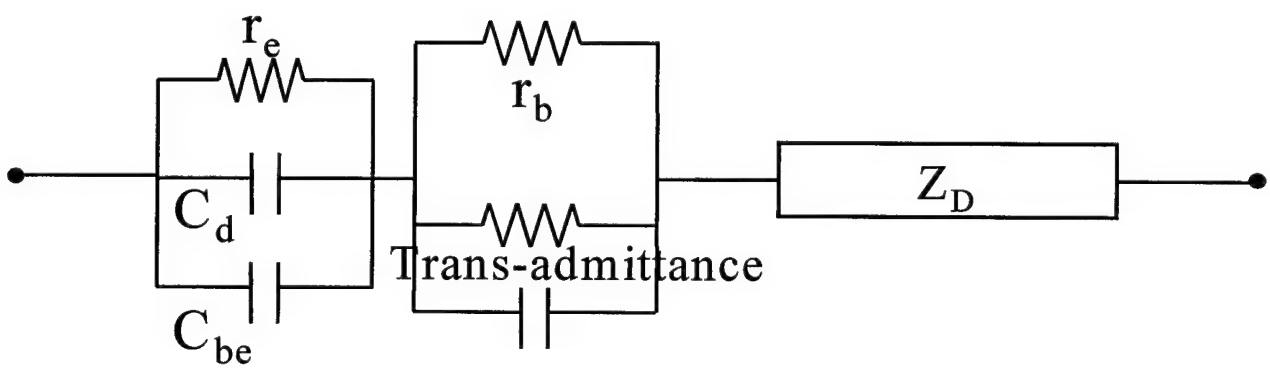
CAPTIONS

Fig. 1. (a) A schematic device structure for BIPOLITT diode. (b) The corresponding small signal equivalent circuit for the BIPOLITT diode. Note that AC junction resistance and AC diffusion capacitance are used.

Fig. 2. The calculated specific AC negative resistance of a BIPOLITT diode designed for 300 ~ 400 GHz at three bias current densities . The key parameters of the device structure are also shown.


n+
E
p+
B (floating)
n
C
Injection region
Drift region

(a)


re
Cd
Cbe
rb
Trans-admittance
ZD

(b)

Figure 1

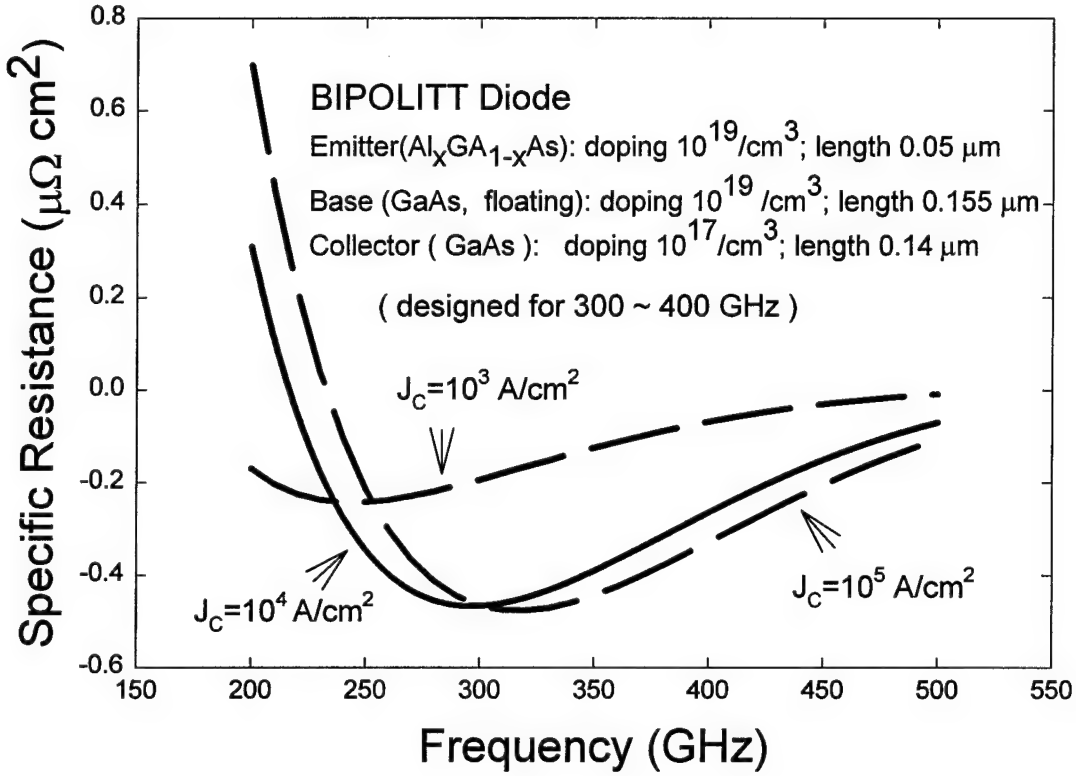

BIPOLITT Diode
Emitter($Al_xGA_{1-x}As$): doping $10^{19}/cm^3$; length 0.05 μm
Base (GaAs, floating): doping $10^{19}/cm^3$; length 0.155 μm
Collector (GaAs): doping $10^{17}/cm^3$; length 0.14 μm
(designed for 300 ~ 400 GHz)
$J_C=10^3$ A/cm^2
$J_C=10^4$ A/cm^2
$J_C=10^5$ A/cm^2
Specific Resistance (μΩ cm^2)
Frequency (GHz)
0.8
0.6
0.4
0.2
0.0
-0.2
-0.4
-0.6
150
200
250
300
350
400
450
500
550

Figure 2

Small Signal Analysis of Bipolar Injection Transit Time Diode (BIPOLITT)

L. Chen and D. S. Pan

Abstract—We have proposed and analyzed a new millimeter and submillimeter wave transit time device named BIPOLITT (Bipolar Injection and Transit Time). The device structure is similar to a Heterojunction Bipolar Transistor (HBT) with a floating base. The relatively longer base is utilized to achieve an injection-phase delay close to 180°. The collector depletion region is used as drift region. As an example, a BIPOLITT diode for 300-400 GHz operation is designed, and its small signal specific negative resistance is calculated to be about $-3\times10^{-7}\,\Omega\cdot\mathrm{cm}^2$

Index Terms—BIPOLITT, HBT, Transit Time

I. Introduction

The negative resistance arising from transit time in the semiconductor diodes was first considered by Shockely [1,2] in 1954. It was shown that when a conduction current pulse is injected into a drift region with a phase delay with respect to the total current, we would have a negative resistance at certain transit angles. Due to the rapid development of FETs and HBTs, the tarnsit time devices such as IMPATT [2,3] are now used in deep millimeter wave frequencies. In submillimeter wave frequencies, there is currently no good solid state source except perhaps the Resonant Tunneling Diode (RTD) [3]. The performance of IMPATT is not satisfactory in deep millimeter wave frequencies and above (with efficiencies lower than a few percent [3]). This low efficiency is primarily caused by the saturation of the ionization coefficients when the electric field is very high [2,3]. As a result, the impact ionization injection cannot be well localized and renders the IMPATT as a low efficiency Misawa diode [2,3].

In this paper, we investigated the possibility to employ a HBT structure with a relatively longer floating base to realize the current injection. The desired phase delay is introduced when the electrons move across the so-called base (injection region) in our designed diode, which is similar to the delay introduced when electrons flow through the base in the Bipolar transistor. That is the reason why we call our diode as the Bipolar Injection Transit Time diode (BIPOLITT). Since the injection mechanism is well localized at the beginning of the drift region, the performance of the BIPOLITT diode can be made much better than IMPATT at deep millimeter wave frequencies and above. Meanwhile, with the mature technology for HBTs, it would be easy to fabricate the BIPOLITT diodes.

Actually, the transit time effects have been long known for the Bipolar transistors. In 1966, J. F. Gibbons [4] pointed out that there may exist a transit time mode oscillation in BJTs because of the excess phase delay due to the transit time effect. In 1988, Sheila Prasad etc. [5,6] have analyzed the High-Frequency characteristics of HBTs and pointed out that the transit-time effect plays a significant role at high frequencies. Their numerical calculation shows that $\mathrm{Re}(h_{22})$ assumes negative values in some portions of the frequency, and the unilateral gain would peak when $\mathrm{Re}(h_{22})=0$. However, those results are not observed in the commercially designed BJTs or HBTs. Based on our analysis, we found out that the main reason is because in those BJTs or HBTs, the transit time effect was not optimized and not sufficient to overcome the parasitic to obtain an overall negative resistance. The detail will be discussed later.

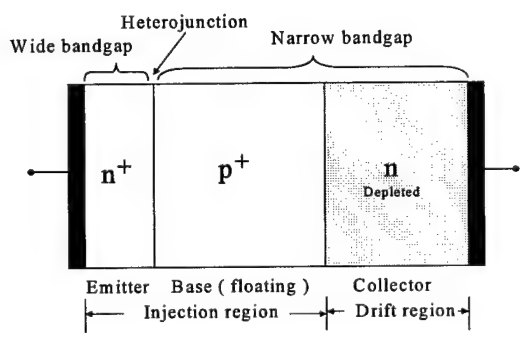


Fig. 1 A schematic device structure for the BIPOLITT diode

II. Device Structure

The basic structure of the proposed BIPOLITT diode is illustrated in Fig. 1. Basically, it looks like a HBT with the base floating. Compared to the regular HBTs, the BIPOLITT has a relatively longer so-called base and a shorter collector. Similar to all transit time devices [2], a BIPOLITT diode consists of an injection region and an adjacent drift region. Electrons are injected from the emitter-base junction into the base region. The AlGaAs/GaAs Heterostructure here is utilized to improve

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the current injection efficiency by reducing the hole current significantly due to the presence of the valence band discontinuity. The neutral base region will provide a phase delay by the diffusion process. The delayed electrons are then injected into the collector depletion region which acts as the drift zone for producing the transit time negative resistance. The HBT technology allows the base doping to become higher than $0^{19}\,\mathrm{cm}^{-3}$ [7] with conductivity therefore larger than $00\,\Omega^{-1}\cdot\mathrm{cm}^{-1}$. With this high conductivity, the dielectric relaxation time [3] is less than 10 fs, and the displacement current is less than 10% of the conduction current up to 1 THz. This means the charge neutrality implicitly assumed in the ambipolar diffusion equation [3] in the base is valid up to 1 THz.

III. SMALL SIGNAL ANALYSIS

It is well known that the ac impedance of the drift region is given as [2,3]

$$Z_d = \frac{1}{j\omega C_d}\left[1 - \frac{\gamma\left(1 - e^{-j\theta_d}\right)}{j\theta_d}\right] \qquad (1)$$

where $C_d = \varepsilon_S/W_d$ is the capacitance per unit area of the drift region, and the transit angle θ_d equals $\omega W_d/v_s$, with W_d the drift region length and v_s the carrier saturation velocity in the drift region.

Both the diffusion and velocity overshoot effects are neglected in Eq. (1). Since Eq. (1) is obtained by an integration of the carriers in the drift region [2,3], the neglect of the diffusion will not be too serious. The inclusion of the velocity overshoot is expected to improve the negative conductance.

The term γ is defined as the ratio of the injection current at the beginning of the drift region to the total ac current and can be written as $\gamma = |\gamma|\cdot e^{-j\phi}$, where ϕ is the so called injection phase delay. For non-zero ϕ, the real part of Z_d will show negative resistance and reach the optimum value when the sum of ϕ and θ_d is equal to 2π.

The calculation of γ depends on the current injection mechanism. As mentioned above, we employ the HBT structure to realize the current injection in the BIPOLITT diode. Assuming a uniform doping and by solving the diffusion equation of electrons in the injection region (neutral base region) at high frequency [8], we can obtain

$$\gamma \cong \frac{(1/r_e)\Gamma\,\mathrm{csch}(\Gamma)}{(1/r_e)\Gamma\coth(\Gamma) + j\omega C_{be}} \qquad (2)$$

where the emitter junction dc resistance $r_e = kT/qI_E$, with I_E as the dc emitter current. The C_{be} is the emitter junction capacitance and ω is the angular frequency. The emitter efficiency is counted as 1 in Eq. (2) since a heterojunction at the emitter junction is used and the hole current is highly compressed. The term Γ is defined as

$$\Gamma = \frac{W_b}{L_{nb}}(1 + j\omega\tau_{nb})^{1/2} \cong (j2.43\,\omega/\omega_b)^{1/2} \qquad (3)$$

where W_b is the thickness of the neutral base, $L_{nb} = \sqrt{D_{nb}\tau_{nb}}$ is the dc diffusion length; τ_{nb} is the base electron life time, and $\omega_b = 2.43\,D_{nb}/W_b^2$ is the base-cutoff angular frequency. Since we are interested in the deep millimeter and submillimeter wave frequencies, $\omega\tau_{nb}>1$ and the term 1 in Eq. (3) can therefore be neglected.

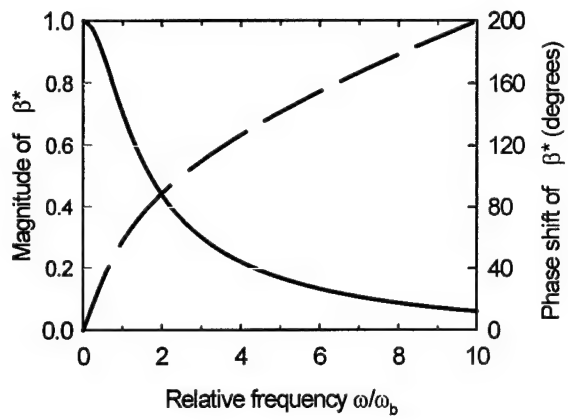

Fig. 2 Frequency variation of β*

Note that if the displacement admittance $j\omega C_{be}$ is negligible when compared with the admittance $(1/r_e)\Gamma\coth(\Gamma)$, Eq. (2) is reduced to the base transport factor $\beta^* \cong \mathrm{sech}(j2.43\,\omega/\omega_b)^{1/2}$ at high frequencies. β^* is the ratio of the electron diffusion current at the end to that at the beginning of the neutral base region, and the frequency response characteristic of β^* is shown in Fig. 2. As we can see, at the base-cutoff frequency ω_b, the magnitude of the β^* is reduced to about 71% with a corresponding phase delay of 58°. However, this phase delay is not sufficient for a good transit time device. More phase delay is required. To obtain a 80° phase delay of β^*, it demands $\omega \cong 8.6\omega_b$ and makes $|\beta^*| \cong 0.09$. This means that the collector injection current can have a phase delay of $80°$ with a magnitude of 9% with reference to the current at the emitter base junction, when the base thickness has a base cutoff frequency of 12% of the operating frequency.

The numerator in Eq.(2) is the trans-admittance of the conduction current at the end of the neutral base region. We

call it a trans-admittance because the voltage is referenced to the emitter-base junction. The denominator in Eq.(2) is the total admittance of the emitter-base junction. The equivalent circuit for the emitter junction can be constructed accordingly. The effect of Ac diffusion capacitance is included in $(1/r_e)\Gamma\coth(\Gamma)$ since the Ac diffusion length is used in Γ [8]. It turns out that the C_{be} is usually small when compared with the Ac diffusion capacitance when the DC biased current is high enough, and only makes the phase delay slightly larger and the magnitude of γ slightly smaller. Therefore, the earlier discussion of the ω dependence of β^* provides a general and simple trend for γ as well. When the injection phase delay is about 80°, we expect an injection efficiency γ of about 10%, which is sufficient for a transit time device.

The equivalent circuit elements for the emitter-base junction compose three parallel elements: depletion capacitance c_{be}, Ac junction resistance r_{be} and Ac diffusion capacitance c_d. The exact equivalent circuit in the base region is very complicated due to the ambipolar diffusion process. However, since the base doping is sufficiently high, it is a very good approximation trepresent it by the base resistance r_b parallel with a voltage-controlled current source $\tilde{\alpha}\upsilon_{be}$, where υ_{be} is the Ac voltage across the emitter-base junction, and $\tilde{\alpha}$ is the trans-admittance as shown in the numerator in Eq. (2).

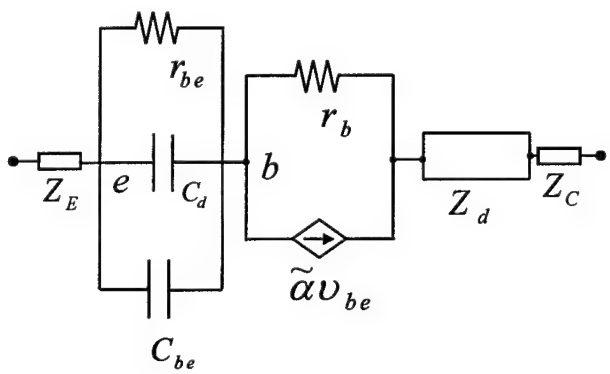

Fig. 3 The small signal equivalent circuit for BIPOLITT

The resultant small signal equivalent circuit including both injector and the drift zone of the BIPOLITT is shown in Fig.3. Z_d is the impedance of the drift region, and Z_C is the impedance for the Ohmic contact of the collector. Z_E is the sum of the Ohmic contact impedance of the emitter and the extrinsic emitter series resistance. It should be pointed out that even though the physics of r_{be} and c_d is clear, we do not give the simplified formula for them, like in the regular analysis in BJTs or HBTs [4-6,8]. In fact, both r_{be} and c_d are dependent of frequencies. However, since both r_{be} and c_d are much smaller than the drift region impedance Z_d, the replacement of r_{be} and c_d by their BJT first order simplified formulae will not cause serious errors in the calculation of the total device impedance.

IV. NUMERICAL RESULTS

According to the device operating principle and the equivalent circuit, we have designed a BIPOLITT for 300 to 400 GHz operation. The parameters for the device is shown in Fig. 4. The thickness of the base region is designed to be $0.155\mu m$, corresponding to a base-cutoff frequency of about 65 GHz. The injection phase delay is about 70° at 400GHz and about 50° at 300 GHz. They are slightly larger than 80° to take advantage of a larger magnitude for γ. The thickness of the collector region is $0.14\mu m$ corresponding to a transit angle of about 80 at 400 GHz. Without including the ohmic contact resistance, the calculated specific resistances of the device are depicted from 200 to 800 GHz for the bias current density of $0^5\ \mathrm{A/cm^2}$ as shown in Fig. 2. The solid line represents the total Ac resistance of the device, while the dotted line represents the resistance of the drift region only. In the designed frequency range, they are approximately $-3\times10^{-7}\Omega\cdot\mathrm{cm}^2$ and $-5\times10^{-7}\Omega\cdot\mathrm{cm}^2$, respectively. These values are good and are comparable to that of the RTD [9].

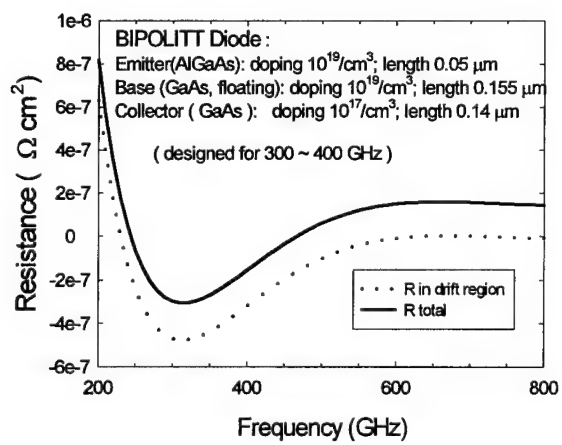

Fig. 4 The calculated specific Ac negative resistance of a BIPOLITT diode

Note that the specific resistance of the base of $0.155\mu m$ thickness with doping $0^{19}\ \mathrm{cm}^{-3}$ is about $.3\times10^{-7}\Omega\cdot\mathrm{cm}^2$, which decreases the total negative resistance by the same value. It is therefore desirable to dope the base more heavily than $0^{19}\ \mathrm{cm}^{-3}$, for example $5\times10^{19}\ \mathrm{cm}^{-3}$, which is possible in today's technology, to decrease the base resistance to be lower than $4\times10^{-8}\Omega\cdot\mathrm{cm}^2$.

At the same time, we must point out that the DC biased current I_E plays a critical role in the BIPOLITT performance. I_E affects the term γ through r_e by changing the weight of the displacement current in the total Ac current. When I_E is high enough, $r_e = kT/qI_E$ becomes very small so that the depletion capacitance c_{be} can be ignored when compared to the Ac diffusion capacitance c_d, since c_d is proportional to $/r_e$ at the first order approximation. Since the Z_d is about $-5\times10^{-7}\Omega\cdot\mathrm{cm}^2$ and the total negative resistance is decreased by the emitter-base junction resistance r_{be} which is equal to r_e at the first order approximation, therefore in order to have a relative large total specific negative resistance, I_E should be larger than $6\times10^4\ A/\mathrm{cm}^2$, which gives $r_e \cong 4.4\times10^{-7}\Omega\cdot\mathrm{cm}^2$. Taking the parasitic Ohmic contact resistance into consideration, it is desired to have I_E larger than $8\times10^4\ A/\mathrm{cm}^2$, which gives $r_e \cong 3\times10^{-7}\Omega\cdot\mathrm{cm}^2$. Meanwhile, a $0^6\ A/\mathrm{cm}^2$ Dc biased current will give $r_e \cong 2.6\times10^{-8}\Omega\cdot\mathrm{cm}^2$ and we can safely ignore the r_{be} compared with Z_d. However, when the Dc current is high, the high current effects happened in Bipolar transistor will occur, which means that a good DC biased current density range in our sample design is from $0^5\ A/\mathrm{cm}^2$ to $0^6\ A/\mathrm{cm}^2$.

Since the total specific resistance is at about $-3\times10^{-7}\Omega\cdot\mathrm{cm}^2$ order, the contact resistance is a big issue in order for the BIPOLITT diode has a good performance. Note that the DC Ohmic contact on GaAS with value less than $3\times10^{-7}\Omega\cdot\mathrm{cm}^2$ is possible to be made in today's technology [10-12]. In the meantime, since our BIPOLITT diode is designed at high frequencies, the shunt capacitance becomes important and decreases the total resistance of the ohmic contact. In our design example, the capacitance is about $30\times10^{-7}\ F/\mathrm{cm}^2$, and at 300 GHz the impedance is about $.8\times10^{-7}\Omega\cdot\mathrm{cm}^2$. Therefore, the total resistance of the Ohmic contact at 300 GHz will be about $0.8\times10^{-7}\Omega\cdot\mathrm{cm}^2$, which allows our BIPOLITT diode to perform with sufficiently specific negative resistance for many applications. Due to the frequency dependence of γ (similar to that of β^*), the BIPOLITT is a wide band transit time device as we can see from Fig. 4.

V. THE BIASING SCHEMES

In this section, we would like to discuss two possible biasing circuits for our BIPOLITT diode as shown in Fig. 5. It is easier to explain by employing the BJT symbol. Basically, both can be view as a Dc current biased BJT operating at base Ac floating mode, the Ac signal drops across the emitter and collector.

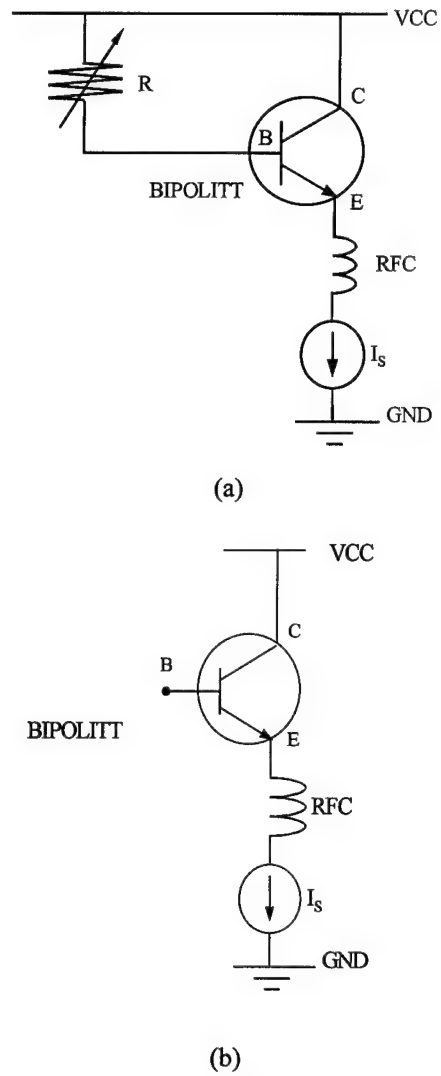

Fig. 5 The biasing circuits for BIPOLITT diode. (a): The voltage across the drift region is adjusted by a variable resistor to control the efficiency and power of the diode; (b): Without the variable resistor, the voltage across the drift region is self-sustained.

In Fig.5(a), the BIPOLITT diode is shown as a BJT. An ideal current source I_S is used to bias the BIPOLITT diode at DC condition. A RF choke (RFC) is used to allow the DC bias, while preventing the current source from degrading the Ac signal.

A variable resistor is used to allow voltage dropping across the collector-base junction to be changeable, therefore, we can adjust the efficiency of the BIPOLITT diode.

Taking our designed BIPOLITT diode as an example. The specific negative resistance is about $-3\times10^{-7}\Omega\cdot\mathrm{cm}^2$. In order to match a 3Ω load, the area for our BIPOLIT diode is about $\times10^{-7}\mathrm{cm}^2$. Biased at $0^5\ A/\mathrm{cm}^2$, the current source will be $0\,\mathrm{m}A$. Meanwhile, according the parameters shown in Fig. 4, the DC common-emitter

current gain β can be made to be about 100 ~ 400. Therefore, the current flowing through the variable resistance R is $0.1 \sim 0.025\,\mathrm{m}A$. If we required the DC voltage across the collector-base junction as $3\,\mathrm{volts}$ to have a good efficiency, the R should be adjusted to be $30 \sim 120\,\mathrm{k}\Omega$. At the same time, the specific negative resistance of the drift region (the collector-base junction) is about $-5\times10^{-7}\,\Omega\cdot\mathrm{cm}^2/1\times10^{-7}\,\mathrm{cm}^2 = 5\Omega$, which is negligible when compared to the much larger value R. Therefore, the Ac signal will not go through the DC biased R branch, but totally flow through the BIPOLITT diode, which makes the BIPOLITT diode as a two-terminal device.

The difference between Fig. 5(a) and (b) is that in Fig. 5(b), the variable resistor R is eliminated. Actually, the effect of the dropout of the R is significant. First, it greatly simplifies the fabrication of diode and circuit. Second, without R, the multi-layer structure (series of BIPOLITT diodes) will be possible for BIPOLITT integration to realize a high power device. However, there exists a big problem for our AlGaAs/GaAs structure: the break down voltage of the device (similar to the BV_{ceo} of BJTs) is as low as about 2 votls since our drift region is at 0.2 μm order. Biased at $0^5\,A/\mathrm{cm}^2$ to $0^6\,A/\mathrm{cm}^2$ DC current density, the voltage across the AlGaAs/GaAs heterojunction (the emitter-base junction) is about 1.4 votls; therefore, there is only about 0.6 volts voltage left for the drift region (the base-collector junction), which is not enough for a reasonable efficiency.

Fortunately, with today's mature technology of HBTs, we can figure out several ways to overcome this drawback by modifying the basic BIPOLITT structure. For example, we can insert a thin insulting region between the base and collector, or employ the heterostructure for the base-collector junction, too. Many works [refreneces???] has shown those two techniques can improve the breakdown voltage substantially. If somehow, we can increase the breakdown voltage to about 4 volts, which leaves 2.6 volts for the drift region to have a good efficiency. Of course, we also can use other materials with higher breakdown voltage instead of GaAs. Nevertheless, the biasing circuit shown in Fig. 5(b) worthies attentions.

VI. DISCUSSION AND CONCLUSION

Our BIPOLITT diode has a comparable performance to the RTDs at millimeter and submillimeter wave frequency range. Meanwhile, because BIPOLITT does not have negative resistance at lower frequency, it will not have the problem of spurious oscillation and bias circuit design problem [13,14] as found in RTD. It can also be integrated in series without the dc instability problem of RTD [15]. It therefore has the potential to be a higher power device than RTDs, and be as one of the best solid state sources in the submillimeter and deep millimeter wave frequency range. A large signal analysis shows the efficiency of the BIPOLITT is about 10% [16], which is comparable to that of the RTD of about 10% in this frequency range.

As mentioned earlier, the major difference between our BIPOLITT diode and the commercially designed BJTs or HBTs [4-6] is that our BIPOLITT diode has a relatively longer base, which introduces a phase delay close to 80°. In fact, the shorter base in the commercially designed BJTS or HBTs is one of the major reasons why the expected negative resistance phenomena are not observed in them. First of all, due to the shorter bases, the commercial BJTS or HBTs generally have base phase delays $\leq 45^\circ$, which is not enough for a good transit time delay. Our simulation [16] found out that at about 30° and 90° base phase delays, the efficiency of a HBT as a negative resistance device are about 1% and 5%, respectively, while reaches about 10% at 80° base phase delay. Second, in order to have the optimum 360° total phase delay, the shorter the base, the longer the collector (the drift) region is. When the collector becomes longer, the diffusion effect will degrade the performance more seriously, which accounts for one of the reasons why our BIPOLITT diode with a shorter drift region is better for the negative resistance device. In the meantime, in the commercial BJTs or HBTs designed to operate at microwave frequency, the negative resistance in the drift region is usually cancelled out by the parasite emitter, base and contact resistance. Our BIPOLITT diode is designed for millimeter and submillimeter wave frequency range, where the parasite resistance are greatly decreased by the no longer negligible shunt capacitance; therefore, the BIPOLITT diode has the potential to be a negative resistance device at millimeter and submillimeter wave frequencies if carefully designed.

In conclusion, we explores the potential of making a good transit time device based on the HBT structure. The proposed BIPOLITT has the great potential to become the solid state source at deep millimeter and submillimeter wave frequencies. It can find applications in millimeter-wave oscillators, amplifiers, and mixers.

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A Post-Shrink MOSFET Design Utilizing Schottky Tunneling Mechanism

J.Y. Liao and D.S. Pan

Abstract—We investigate a very small transistor design utilizing Schottky tunneling mechanism. The structure with a metal/semiconductor Schottky junction replacing the source of a conventional MOSFET is extensively analyzed and simulated. A number of simple analytical formulae to implement the design are derived. Very good transistor characteristics are obtained

Index Terms—MOSFET, tunneling

I. Introduction

As the device development advances toward sub-100nm regime, there exist a number of significant technical barriers to the extension of current technology. Material properties and fundamental operating principles of MOSFETs will soon become the limiting factors of device scaling [1]. Furthermore, non-scaling parameters such as threshold voltage (V_T) and subthreshold current (I_{OFF}) are still challenging the sub-100nm technology. Moreover, fabrication technology, in an effort to keep up with the extraordinary advancement of integrated circuits (IC), is facing serious problems such as random processing defects and interconnection. To overcome these difficulties, research efforts have been directed toward the investigation and development of alternative, non-conventional MOSFET structures [2]. These devices should offer not only high transconductance but also relatively simple fabrication procedures to minimize parasitic effects. Structures such as Schottky barrier source and drain MOSFETs have been proposed [3-5].

The voltage loss at the Schottky barrier between the source and the channel has been a major concern in the development of Schottky source/drain devices for low voltage applications. As device engineers are confronted with complications associated with ultra-small transistors, experiments have demonstrated a favorable possibility of velocity overshoot in very short devices under low voltage operation [6]. For devices with gate length below 0.1μm, electron speed at the source edge has become the most important performance factor [6,7]. Electrons penetrating the Schottky barrier possess significantly higher speed than the velocity saturation value, since they are oriented directly into the channel. Also, contact resistance is *eliminated* because electrons enter the channel directly from the metal. Thirdly, because tunneling phenomenon is a majority carrier effect, issues such as inversion layer broadening can be neglected, and the turn-off behavior of transistors is characterized by thermionic tunneling. Moreover, no gate voltage is needed to change the surface potential and to offset the depletion-layer charge; space charge is induced by the corner electric field at the source-channel interface, and independent of channel doping. The combination of the above-mentioned offers a beneficial tradeoff for the voltage drop loss at the source edge.

Approaches in utilizing tunneling barrier in MOSFET operation have been reported [4,8]. In these MOSFETs where tunneling injectors are employed, the source is typically a reverse-biased Schottky barrier. The Schottky barrier depletion width at the reverse-biased condition is dependent on the gate bias; this dependence results in the three-terminal transistor effect: the drain current being controlled by the gate bias. In other words, when a positive gate voltage is applied, the tunneling barrier at the source-channel interface becomes narrower, resulting in the enhancement of tunneling mechanism.

In research work where a Schottky-semiconductor interface has been employed to both the drain and source of the MOSFET, the reported drain current is low (in the order of μA/μm), and the transistor does not leave triode mode [5]. Furthermore, subthreshold behavior of these devices is not characterized. Although Schottky barrier transistors do offer a fabrication advantage over conventional MOSFETs, researchers have to address the enhancement of transconductance and transistor characteristics, as these are the major concerns for the development of tunneling transistors for IC applications.

II. Device Structure

The structure proposed in this research work is similar to a MOSFET, with metallic termination at the source. The significant features are the physical dimensions: the gate length varies from 300Å to 500Å *in order to enhance Schottky tunneling mechanism*, and the thickness of the active layer is generally ⅓ (100Å in the structure proposed in Fig. 1) of the gate length for large current handling capability. This structure consists of an n-doped semiconductor as the active layer, an insulated gate, and intrinsic substrate which is necessary to provide electrical

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isolation between neighboring electrodes. To characterize tunneling mechanism in modeling and simulation, silicon-germanium parameters are employed. *For better device isolation and reduction in substrate leakage and parasitic capacitances [2]*, a backside oxide is sandwiched between the active thin film and the substrate, similar to a Silicon-on-Insulator (SOI) MOSFET.

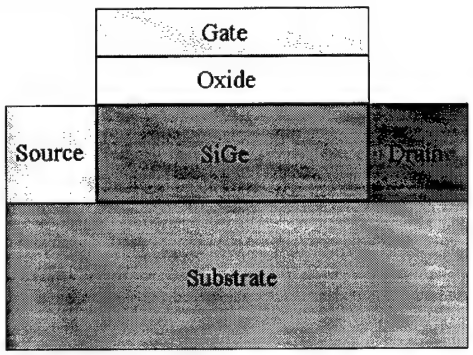


Figure 1. Schematic structure of a Schottky source MOSFET. t_{ox} (=50Å) is the gate oxide thickness, t_{Si} (=100Å) the active layer thickness, and L (=300Å) the gate length.

III. Simulation Method

ATLAS 2-D device simulator program by Silvaco is utilized in the simulation of proposed device structures. The simulator does not provide a model for Schottky tunneling but for interband tunneling. However, because of the fact that both tunneling mechanisms are characterized as functions of local electric fields [9], the interband tunneling method can be modified to accommodate the modeling of Schottky tunneling mechanism.

Two-dimensional numerical simulation is performed on a Schottky barrier MOSFET with metallic material replacing both the conventional source and drain. Because electrons generated at the source edge have to overcome the Schottky barrier at the drain edge, the device suffers a delayed turn-on. A voltage applied to lower the drain barrier is required before large amount of electrons can be collected by drain. The transistor enters saturation mode at a higher drain voltage, and the delay in turn-on is unfavorable toward low voltage operation. In order to achieve a better transistor characteristic where the device is saturated at a low drain bias, the transistor with the drain remaining a perfect Ohmic contact is extensively simulated.

IV. Analysis of Tunneling Current

Generally, the Schottky tunneling current density discussed in previous research work [4] is expressed in an integral form, and the dependence of current on transverse momentum was not considered in the derivation. *We attempt to include the measure of significant range of transverse momentum in our discussion*, and provide a simple analytical expression for the Schottky tunneling. In this section we will discuss the derivation of tunneling currents, current dependence on electric fields, approximation of electric fields, and subthreshold behavior.

Derivation of Tunneling Currents

To better understand and analyze the tunneling currents, we categorize the total current into four components according to the energy range within which tunneling occurs: 1.) Schottky tunneling current for tunneling between the metal Fermi level and the edge of semiconductor valance band; 2.) Band-to-band tunneling current for tunneling from the valance band edge to infinity; 3.) Thermionic tunneling current for tunneling between metal Fermi level to the edge of the conduction band; and 4.) Over-barrier thermionic tunneling current for tunneling from the conduction band edge to infinity. For significant interband tunneling to occur, a large drain voltage must be applied to reverse bias the junction so that the conduction band is lowered below Fermi level. Moreover, electrons must travel a distance to reach valance band edge before starting to tunnel, and the electric field at the location for interband tunneling to occur should also be sufficiently high. *Because of these constraints, interband tunneling is not discussed in detail in this paper.*

Consider a metal-semiconductor interface as illustrated in Fig. 2. Electrons with energy above metal Fermi level are trying to tunnel through the barrier width and enter the conduction band. When a small bias is applied to the drain, the barrier at the drain side is lowered, and electrons are collected. When the drain bias reaches approximately the difference between the metal Fermi level and the semiconductor valance band edge, the integration of the number of electrons constitutes the total Schottky tunneling current. Additional depletion width narrowing beyond this drain voltage becomes negligible, and further increase in drain bias does not result in significant current increase. Therefore, the device enters saturation mode beyond this point.

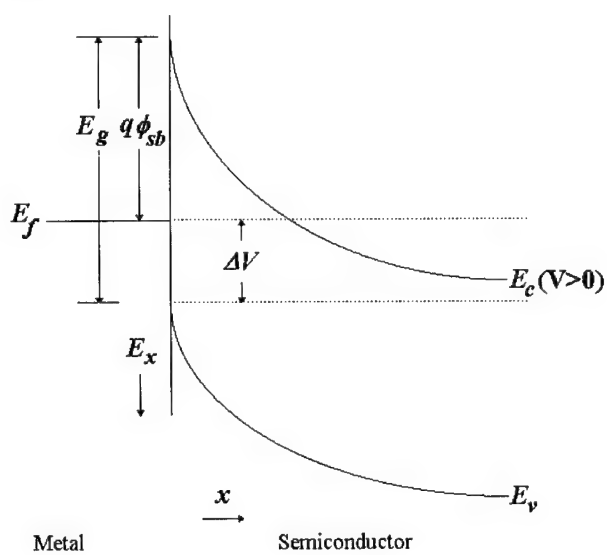


Figure 2. Schematic diagram of Schottky barrier and the definitions used in the current derivation.

From the derivation of electrons tunneling through a triangular barrier, and the theory of tunneling with momentum being conserved [2,9], the incident current density is expressed as

$$J_{tSCH} = \frac{K}{2} \int_0^{(E_g - q\phi_{sb})} \exp\left(\frac{-P_{SCH}}{\xi_0} \left(1 + \frac{E_x}{q\phi_{sb}}\right)^{3/2} \right) \frac{Q_{SCH}\xi_0}{\left(1 + \frac{E_x}{q\phi_{sb}}\right)^{1/2}} dE_x$$

The integration to determine Schottky current density is taken over the energy range from the metal Fermi level (E_x is defined 0 at this level) to the edge of the semiconductor valance band ($E_g - q\phi_{sb}$). A close form of the current expression can be closely estimated by Taylor expansion. Numerical analysis shows that the simplified expression is only slightly deviated from the original equation, and it provides a good approximation for Schottky tunneling current. For large bandgap material (e.g. Si) where tunneling is difficult, a large electric field is required to achieve a large current density for useful applications (Table.1).

For Si- or SiGe-Al interfaces, Schottky barrier height is roughly ⅔ of the semiconductor bandgap. We can further simplify the expression of J_{tSCH} as

$$J_{tSCH} \approx \frac{KQ_{SCH}E_g}{6P_{SCH}} \xi_0^2 \exp\left(-\frac{P_{SCH}}{\xi_0}\right)$$

This is a simple formula to implement the transistor design utilizing Schottky tunneling mechanism at the source-channel edge.

Max ξ_0 (MV/cm)	Si Max J (A/cm^2)	SiGe Max J (A/cm^2)
2	500	1.22e6
3	2.7e4	4.66e6
4	2.3e5	9.86e6

Table 1. Schottky tunneling current density for Si- and SiGe-Al parameters under maximum electric field.

Current Dependence on Electric Fields

From simulations, the magnitude of the parallel electric field is varying with position, and can be approximated with a simple exponentially decaying function with a decay parameter of t_{ox}:

$$\xi(x) = \xi_0 \exp\left(\frac{-x}{t_{ox}}\right)$$

In order words, when the distance of tunneling reaches beyond oxide thickness, the electric field becomes too small, and tunneling current generated under this electric field is negligible. Changing the integration variable at $x = \frac{E_x}{q\xi_0}$, we can re-write the current density as

$$J_{tSCH} = \frac{K}{2} \int_0^{(E_g - q\phi_{sb})} \left\{ \exp\left(\frac{-P_{SCH}}{\xi_0 \exp\left(\frac{-E_x}{q\xi_0 t_{ox}}\right)} \left(1 + \frac{E_x}{q\phi_{sb}}\right)^{3/2} \right) \frac{Q_{SCH}\xi_0 \exp\left(\frac{-E_x}{q\xi_0 t_{ox}}\right)}{\left(1 + \frac{E_x}{q\phi_{sb}}\right)^{1/2}} dE_x \right\}$$

Comparison of Schottky tunneling currents with and without electric fields being dependent on position is illustrated in Fig. 3.

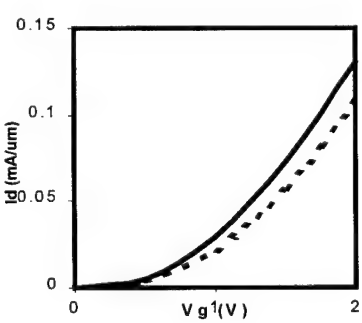


Figure 3. Calculated maximum Schottky tunneling currents with SiGe parameters. $V_{ds} = 0.5V$. t_{id} = 50Å. Dependence of electric field on position is included in dashed line.

Thermionic Currents

Electrons with all energy levels are also tunneling through Schottky barrier. These electrons contribute to the thermionic current. The thermionic current consists of two components: thermionic tunneling current integrated from the metal Fermi level to the edge of the Schottky barrier height, and over-barrier thermionic current integrated from the edge of the Schottky barrier height to infinity. Over-barrier thermionic current density, $J_{OVITHER}$, is given by [2]

$$J_{OVITHER} = A^* T^2 \exp\left(-\frac{q\phi_{sb}}{kT}\right)$$

where A^* is the effective Richardson constant for thermionic emission. For device operated at room temperature, $J_{OVITHER}$ is negligible.

The thermionic tunneling current component is proportional to the quantum transmission coefficient multiplied by the occupation probability in the semiconductor and the unoccupied probability in the metal. The tunneling probability, however, is significantly smaller for electrons with energy below Fermi-level, although they are to tunnel through a narrower barrier. This small

amount of current is also dependent on the electric field. The current density expression for the thermionic component is derived with a similar approach to that of Schottky tunneling current, with modification of the integration boundaries and tunneling constants.

$$J_{tTHER} = \frac{K}{2}\int_0^{q\phi_{sb}} F(E_\chi)\exp\left(\frac{-A_{THER}}{\xi_0}\right)B_{THER}\xi_0 dE_\chi$$

where

$$A_{THER} = \frac{4\sqrt{2}m^{*1/2}\left(E_\chi\right)^{3/2}}{3q\hbar}, B_{THER} = \frac{4\sqrt{2}q\hbar}{3\pi m^{*1/2}\left(E_\chi\right)^{1/2}}$$

and $F(E_\chi)$ is the occupancy factor given by:

$$F(E_\chi) = \frac{1}{1+\exp\left(\frac{q\phi_{sb}-E_\chi}{kT}\right)}$$

The integration is taken (with E_χ positive upwardly) from Fermi level (defined 0) to the edge of the conduction band. I_{tSCH} is dominant under small gate bias, and contributes to the total current at high gate voltages.

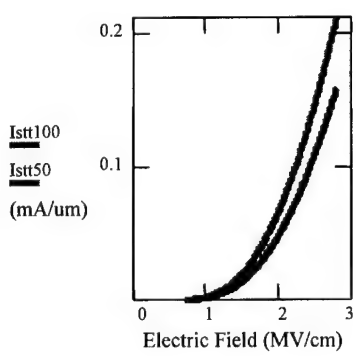


Figure 4. Total current ($I_{TOTAL} = I_{tSCH} + I_{tTHER}$) versus electric field with SiGe-Al parameters. t_{Si} is 100Å in Istt100, and 50Å in Istt50.

Threshold Voltage

For conventional MOSFETs, the threshold voltage, V_T, is defined as the gate bias when diffusion current is equal to the conduction current. In Schottky source/drain MOSFETs, these are the thermionic current and the Schottky tunneling current, respectively. The ON current, I_{ON}, can be considered as the current flowing when Schottky tunneling current is equal to thermionic current, or when current is increased a decade higher than the thermionic current under no gate bias. With numerical approximation, a close form of J_{tTHER} is expressed as

$$J_{tTHER} \approx KQ_{SCH}\left(q\phi_{sb}\right)\xi_0 \exp\left(-\frac{q\phi_{sb}}{4kT}\right)\exp\left(-\frac{3P_{SCH}}{4\xi_0}\right)$$

Consider the first definition. While I_{tSCH} is integrated up to the distance roughly equal to t_{ox} (obtained from simulation and two-dimensional analysis), I_{tTHER} is integrated along the entire active layer thickness. Solving for ξ_0 when $I_{tTHER} = I_{tSCH}$, we arrive at the following expression:

$$\frac{4\xi_0}{P_{SCH}}\exp\left(-\frac{P_{SCH}}{4\xi_0}\right) \approx \frac{16t_{Si}}{t_{ox}}\exp\left(-\frac{q\phi_{sb}}{4kT}\right)$$

Numerical solution with geometry parameters yields

$$\xi_0 \approx \frac{P_{SCH}}{4}$$

If we consider I_{ON} as an order of magnitude higher than I_{tTHER} at $V_{gs} = 0V$, equating the two currents yields

$$\frac{\xi_0^{\,2}}{P_{SCH}^{\,2}}\exp\left(\frac{-P_{SCH}}{\xi_0}\right) \approx \frac{40\kappa\left(-V_{FB}\right)t_{Si}}{P_{SCH}t_{ox}^{\,2}}\exp\left(\frac{-q\phi_{sb}}{4kT}\right)\exp\left(\frac{3P_{SCH}t_{ox}}{\kappa V_{FB}}\right)$$

The solution with proper geometric parameters gives similar results as in first case. This is the threshold electric field, and the corresponding threshold voltage is given by

$$V_T = \frac{t_{ox}}{\kappa}\frac{P_{SCH}}{4} + V_{FB}$$

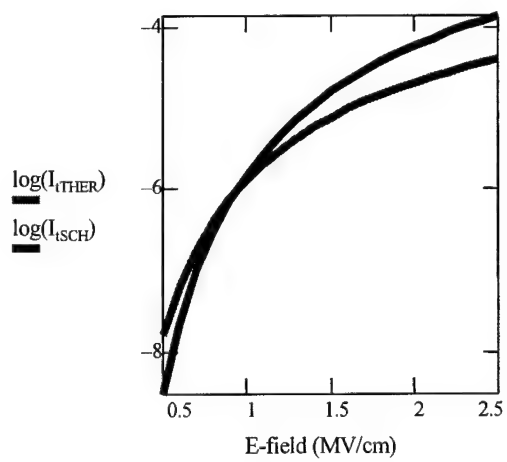


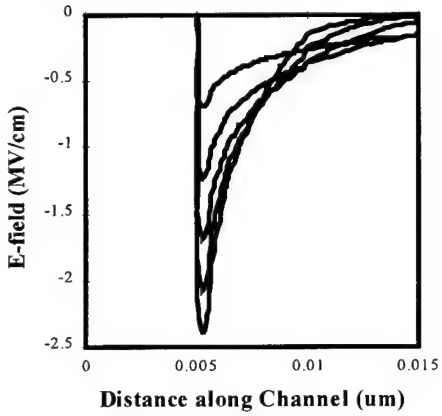
Figure 5. Calculated currents versus electric field. t_{ox} =50Å.

Electric Fields

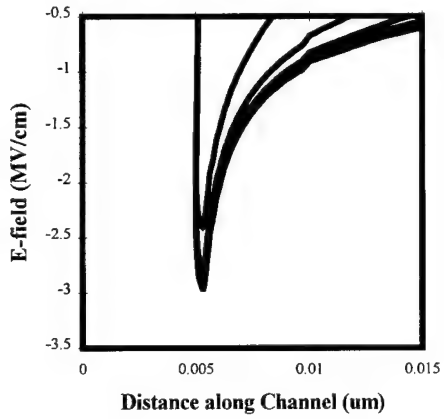
To understand the electric field distribution is the most important step in analyzing Schottky tunneling mechanism, since it is characterized as a function of local electric field. The electric field (ξ_0) at the corner of the source-channel interface below gate oxide strongly affects the current density. For simplicity, the electric field is expressed as:

$$\xi_0 \approx \kappa\frac{V_{gs}-V_{fb}}{t_{ox}}$$

A correction factor, κ, necessary to modify the field expression, is dependent on the geometries of t_{ox} and t_{Si}. Parallel electric field distribution against distance along the channel under different gate biases is plotted in Fig. 6(a). For all figures plotted against the distance along the channel, the device dimensions are described in Fig. 1 unless otherwise noted. Cross-section is obtained 1Å into the active thin film from the Si/SiO_2 interface.



(a) V_{ds}=0, V_{gs} steps from 0 to 2V.



(b) V_{gs}=0, V_{ds} steps from 0 to 2V.

Figure 6. Simulated parallel electric fields along channel. The varying voltage increases evenly with 0.5V per step.

The electric field is not only modulated by V_{gs} but affected by V_{ds} as well. Figure 6(b) illustrates the drain influence on the parallel electric fields at V_{gs}=2V. The phenomenon is possibly resulting from the two-dimensional effect. To understand the dependence of drain voltage on the maximum corner electric fields, we employ the two-dimensional analytical model for fully depleted SOI MOSFETs proposed by Young [16], and modify the boundary conditions to accommodate the Schottky barrier source. It should be noted that when drain is biased beyond depletion, space charge effects should also be considered and included in the calculation. The variation of electric field due to generated carrier space charge is more significant at smaller drain biases (Fig. 7).

The derivative of potential distribution with respect to the position in the tunneling direction, yields the parallel electric field expression. For the device structure in Fig. 1 with a backside oxide of thickness (t_{box}) of 50Å sandwiched between the active silicon layer and the substrate, the maximum electric field can be approximated by

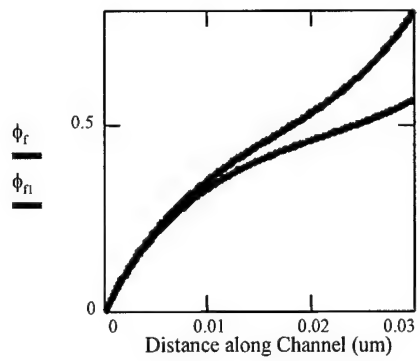
$$\xi_{0f} \approx \frac{-1}{\sqrt{3}t_{ox}}\left(0.94V_{gs}' + 0.064V_{ds}'\right) + \xi_{0FB}$$

where $\xi_{0FB} = 0.2^{MV}/_{cm}$ from simulations.

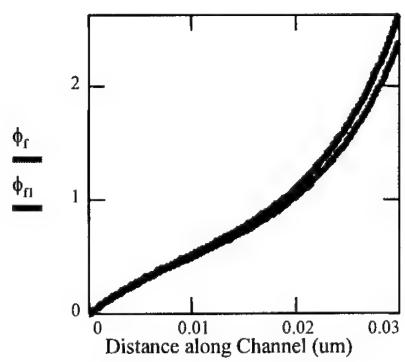
If t_{ox} is 30Å,

$$\xi_{0f} \approx \frac{-0.41}{t_{ox}}\left(0.97V_{gs}' + 0.054V_{ds}'\right) + \xi_{0FB}$$

where $\xi_{0FB} = 0.15^{MV}/_{cm}$.



(a) V_{ds}=0.2V.



(b) V_{ds}=2V

Figure 7. Calculated potential distribution (V) versus distance along channel under Si/SiO_2 interface from two-dimensional model. Space charge effect is included in ϕ_{f1}. Gate is unbiased.

V_{gs} (V)	Max ξ_0 ($^{MV}/_{cm}$) (simu.) t_{ox} = 50Å	Max ξ_0 ($^{MV}/_{cm}$) (calc.) t_{ox} = 50Å	Max ξ_0 ($^{MV}/_{cm}$) (simu.) t_{ox} = 30Å	Max ξ_0 ($^{MV}/_{cm}$) (calc.) t_{ox} = 30Å
0	0.74	0.78	0.8	0.84
0.5	1.32	1.32	1.49	1.50

1	1.87	1.86	2.15	2.17
1.5	2.36	2.41	2.68	2.83
2	2.79	2.95	3.15	3.49

Table 3. Simulated and calculated maximum corner electric fields for different t_{ox} of an SSOD device. $V_{ds} = 0.5V$. A deviation of the calculated values from the simulated is observed at high gate biases. This is because of electric fields being less dependent on V_{ds} beyond saturation.

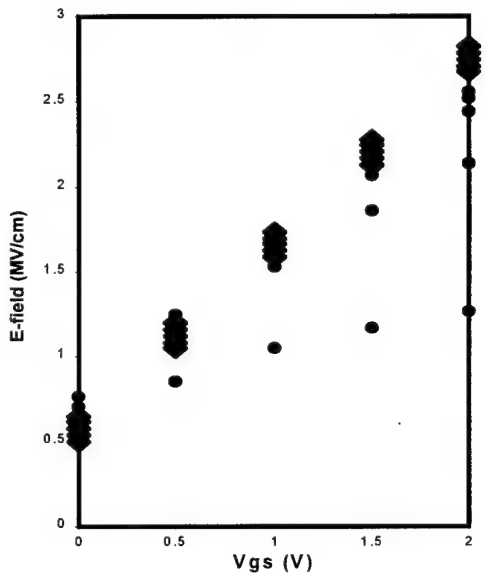
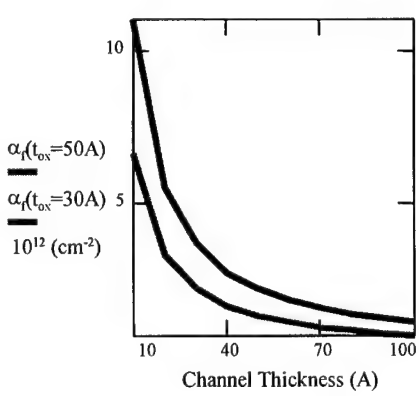


Figure 8. Simulated (dots) and calculated (rhombuses) maximum corner electric fields of an SSSD device. t_{ox}=50Å.



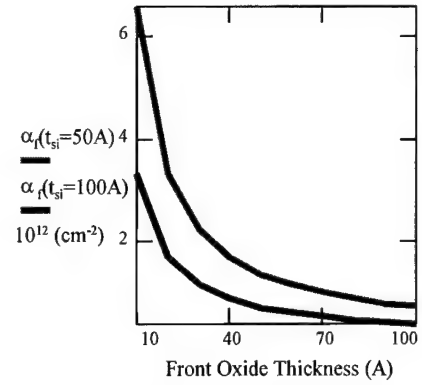


Figure 9. Calculated dependence of α_f on t_{Si} and t_{ox}. t_{box}=5000Å.

Figure 8 illustrates the simulated and calculated ξ_0 versus V_{gs} under different V_{ds}. A significant difference between the simulated and calculated ξ_0 is observed at small V_{ds}. Because at small V_{ds}, electrons penetrating the source barrier are blocked by the Schottky barrier at drain, the accumulation of electrons confined by the barrier well (Fig. 11(a)) lowers the electric field at the source-channel interface. This phenomenon is not included in the two-dimensional derivation. However, the equations still provide a close estimate of ξ_0 when the device saturates. In fact, the lowered electric field at small V_{ds} results in small current flow, and therefore superior turn-off behavior.

Intuitively, ξ_0 would be inversely proportional to t_{ox}; i.e., when t_{ox} is reduced from 50Å to 30Å, ξ_0 should increase accordingly. However, simulation and calculation do not agree with the ideal expectation. This is because of the fact that in additional to t_{ox}, other geometric parameters such as channel thickness (t_{Si}) and backside oxide thickness (t_{box}) are also affecting the magnitude of ξ_0. These terms are expressed in α_f, and grouped as the correction factor κ. The following figures show the geometric dependence of α_f. Γ_f, a parameter which characterizes two-dimensional effect, is the product of $\alpha_f^{1/2}$ and the channel length. The larger Γ_f, the lesser dependence of potential and electric fields on two-dimensional geometry. Numerical calculation shows that with given channel length, short channel effect is significant when t_{Si} or t_{ox} is reduced (Fig.9).

Integration Distance

Gate oxide thickness is not only an important parameter for approximating maximum electric field at the corner of the source-channel interface, but also assumed as the integration distance for current estimation along the direction perpendicular to the Si/SiO_2 interface.

The tunneling current $\left(mA/\mu m\right)$ is obtained by integrating the current density along the distance perpendicular to the Si/SiO_2 interface. The determination of t_{id} depends strongly on the decay of ξ_0. As ξ_0 decays to a certain value when tunneling under this electric field becomes less significant, this will be the upper integration limit. There are a few possible estimates of t_{id}. It is simplicity to assume that the electric field decays with the decay factor equivalent to the gate oxide thickness; therefore, t_{id} equals to t_{ox}. This assumption provide an acceptable approximation of drain current for t_{ox}=50Å. When t_{ox} is reduced, we expect much larger drain current due to the increase in electric field. However, as t_{id} is limited by t_{ox}, the total current may not be much higher than that for thicker gate oxide.

V. Simulation Results

The analysis is compared with the simulation results for a better understanding of Schottky tunneling mechanism. Structures with Schottky source and Schottky or Ohmic drain are simulated. Effects of geometric dependence are also included. I-V characteristics, threshold voltage, transconductance and cutoff frequencies are discussed in detail.

Transistor Characteristics of Schottky barrier Source and Drain (SSSD) MOSFETs

The structure with Schottky barrier source and drain (SSSD) was simulated. The drain current is plotted against a sweeping drain voltage in Fig. 10, with gate bias stepping from 0 to 2V. A delayed turn-on and the near-saturated I-V curves are the major characteristics observed in this simulation. The delay in turn-on is due to the voltage loss at the Schottky barrier between the drain and the channel, when the high speed electrons generated by tunneling mechanism at the source-channel interface have to overcome the barrier before entering drain (Fig. 11(a)). Although tunneling width narrows as V_{gs} increases, electrons penetrating the source barrier are blocked by the drain barrier when V_{ds} is small. The drain barrier has to be lowered for a large amount of electrons to be collected by drain (Fig. 11(b)). A slope in transistor characteristics beyond saturation is observed in the simulation. This is attributed to interband tunneling, when electrons begin to tunnel from valance band directly into conduction band at sufficiently high drain voltage.

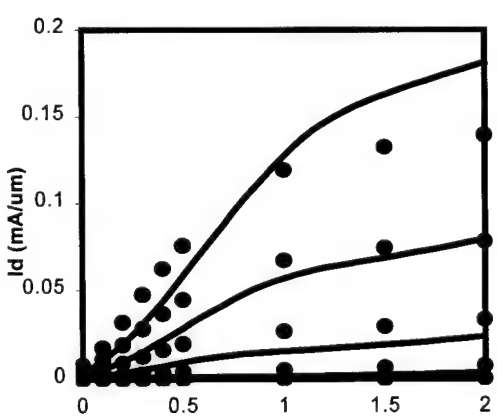


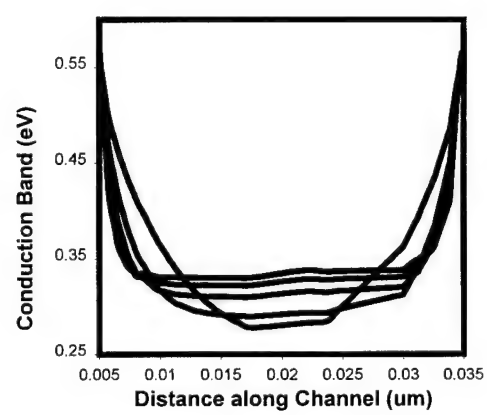
Figure 10. Simulated (solid lines) and calculated (dotted lines) transistor characteristics of an SSSD MOSFET. V_{gs} steps evenly from 0 to 2V.

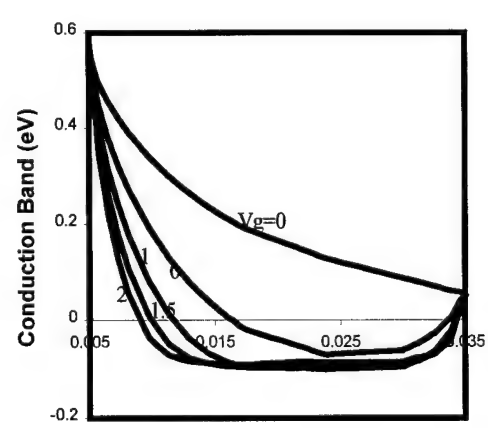
The resulting electric field (Fig. 12(b)) at V_{ds}=0 is significantly lowered due to the confinement of electrons between the two Schottky barriers. The current flowing is the thermionic tunneling current under high electric fields. It is also observed that, although the drain current exhibits an exponential increase after turn-on, the device will not reach saturation until sufficiently high drain voltages (1V is necessary in this simulation.) For it is necessary to lower the conduction band edge of the drain edge to the level of the metal Fermi level before electrons can be collected. $V_{ds,SAT}$ is approximately equal to E_g/q; i.e., after the conduction band edge at drain is lowered to the level as the valance band edge at source, further increase in drain voltage will not result in significant increase in current.

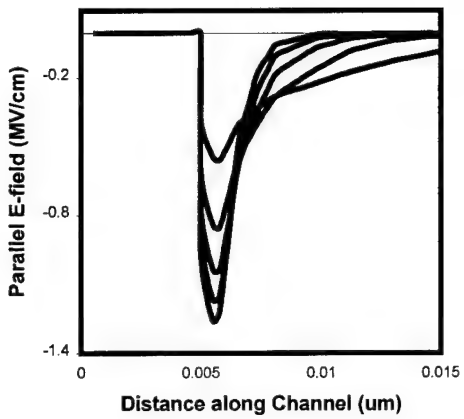
(a) V_{ds}=0.

(b) V_{ds}=0.5V.

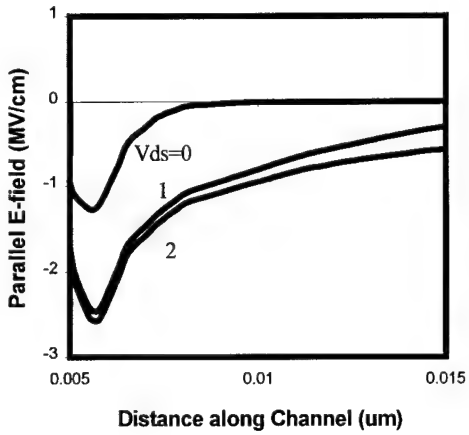
Figure 11. Simulated conduction band bendings of an SSSD MOSFET. V_{gs} increases evenly from 0 to 2V with 0.5V per step.







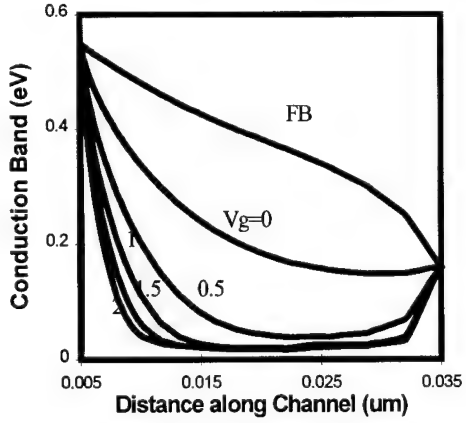
(a) V_{ds} =0, V_{gs} steps from 0 to 2V.



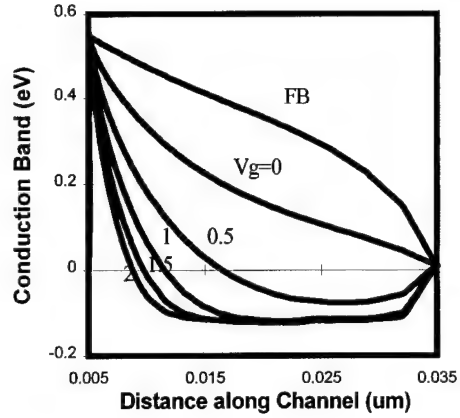
(b) V_{gs} =0, V_{ds} steps from 0 to 2V.

Figure 12. Simulated parallel electric fields of an SSSD MOSFET.

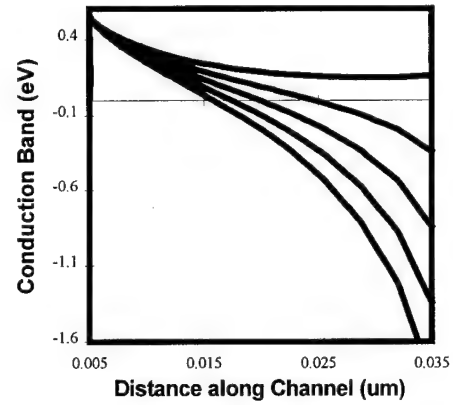
Transistor Characteristics of Schottky Source Ohmic Drain (SSOD) MOSFETs



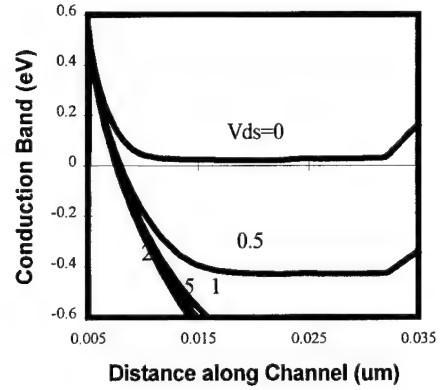
(a) V_{ds} =0, V_{gs} steps from 0 to 2V.



(b) V_{ds} =0.15V, V_{gs} steps from 0 to 2V.



(c) V_{gs} =0, V_{ds} steps from 0 to 2V.



(d) V_{gs} =2V, V_{ds} steps from 0 to 2V.

Figure 13. Simulated conduction band bendings of an SSOD MOSFET along channel under different bias conditions. $V_{gs} = V_{fb}$ is included in (a) and (b). The varying voltage increases evenly with 0.5V per step.

To improve saturation characteristics for low-power IC applications, simulations were performed on a modified structure with drain remaining a perfect Ohmic contact. The profiles of conduction band bendings along channel are illustrated in Fig. 13(a) with drain unbiased. As gate bias is equal to the flatband voltage, the potential barrier is tall enough to block electrons flowing from the source to the drain. When gate bias is more positively increased,

electrons at the Si/SiO_2 interface are induced, and a much thinner tunneling barrier is formed between the source and the channel, therefore resulting in a significantly enhanced channel conductance. Under this condition, current starts to flow when a small drain bias is applied (Fig. 13(b)).

A small barrier at the drain which results from the built-in potential between two differently doped semiconductor regions has to be overcome before current enters drain (Fig. 13(a)). When a moderate drain bias is applied, current starts to flow, and increase linearly with V_{ds}. When V_{ds} reaches beyond $\left(\frac{E_g}{q} - \phi_{sb}\right)$ further increase in V_{ds} will not result in linear variation in current. The device enters saturation mode at this V_{ds}. The device enters saturation when the drain bias reaches approximately 0.5V (Fig. 15).

It is also observed that when drain is biased beyond certain range, its effect on the depletion width narrowing becomes insignificant (Fig. 13(d)). This is because of the fact that the dependence of electric field is on drain voltage is modulated by the channel length, which is much larger than the gate oxide thickness.

The effect of different channel thicknesses is also simulated (Fig. 14). However, the difference in drain current cannot be attributed only to the same thermionic tunneling current density integrated up to t_{Si}. For in reducing t_{Si}, the interdependence of geometric parameters change, and the potential and electric field distributions also vary, according to the two-dimensional analytical modeling. Numerical calculation shows that the corner electric field and tunneling current are enhanced at t_{Si} = 50Å.

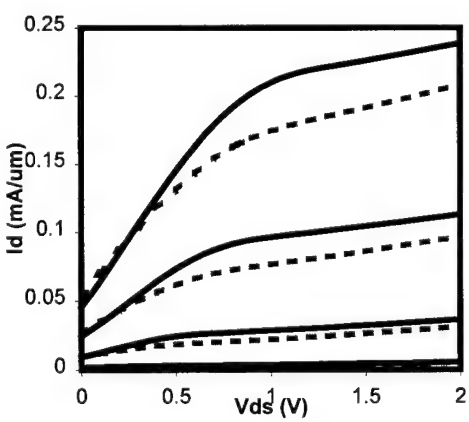


Figure 14. Simulated transistor characteristics of a SSOD MOSFET with germanium as the active layer. V_{gs} increases evenly from 0 to 2V with 0.5V per step. The only varying parameter is t_{Si}: 100Å (dotted lines) and 50Å (solid lines).

It is also noticed that a large amount of current exists with unbiased gate. This could be explained by the fact that the built-in potential at the drain-channel interface induces an electric field which might be high enough for interband tunneling to occur before gate bias is applied. This provides a possible explanation of drain current when V_{ds}=2V and V_{gs}=0V (Fig. 13(c)).

The transistor characteristics are illustrated in Fig. 15. The solid lines depict the simulated family curves and the dots are the calculated drain currents with maximum electric fields extracted from simulation. With these modifications, it is observed that the values of total drain currents calculated with the theoretical expression correspond to the saturation currents in Fig. 15. It should also be noted that when $V_{ds} = 0$, the electric field drops significantly fast, reaching e^{-1} of its maximum value at the location approximately ½ of t_{ox} beneath the Si/SiO_2 interface, where t_{ox} is the decay factor. Therefore, the total tunneling current under this condition is integrated up to ½ of t_{ox}. These calculated values are included. When V_{ds} is smaller than $V_{ds,SAT}$, the drain current is controlled by both V_{gs} and V_{ds}. As the device enters saturation mode, the dependence of the drain current on V_{ds} becomes less significant, and V_{gs} is modulating the ON-OFF currents of the transistor. These are similar to the typical *I-V* characteristics of conventional MOSFETs, and ideal for low-power IC applications.

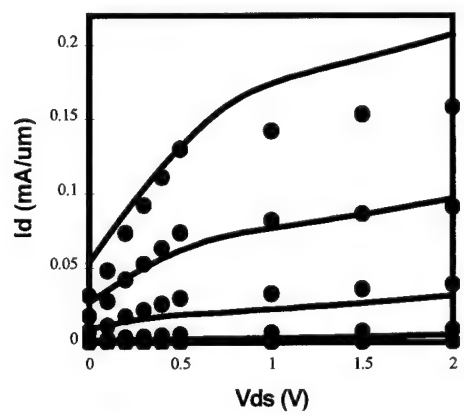


Figure 15. Simulated transistor characteristics of an SSOD MOSFET. Simulated (solid lines) and calculated (dotted lines) I-V characteristics with V_{gs} stepping evenly from 0 to 2V.

Subthreshold Behavior

By defining the ON state at the condition where Schottky tunneling current equals thermionic current, we derive a simple approximation for threshold voltage. It is expressed in terms of Schottky barrier height, effective mass, front oxide thickness, and flatband voltage. With SiGe-Al parameters, V_T is roughly estimated to be 0.5V, which corresponds to the ON position (Fig. 16). A V_{gs} of approximately 1V is necessary to raise the drain current by

3 decades when V_{ds}=0.5V. Figure 17 shows the subthreshold swing versus gate bias under different drain voltages. At higher V_{ds}, it is more difficult to turn off the device, as a larger S is required.

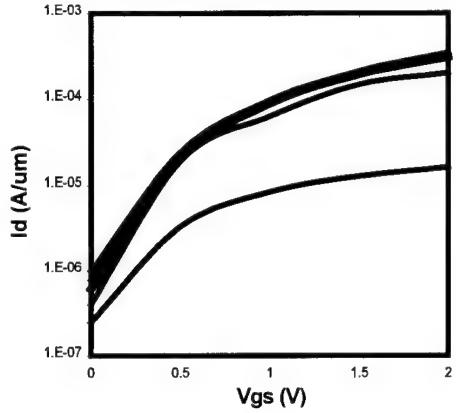


Figure 16. Calculated subthreshold characteristics for an SSSD device with V_{ds} stepping from 0 to 2V.

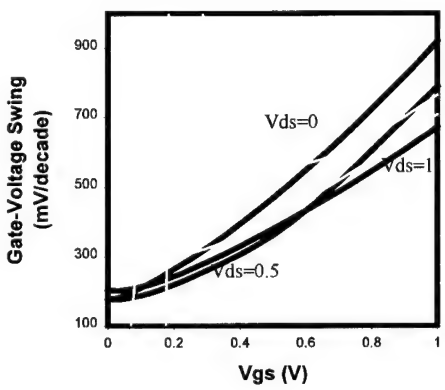


Figure 17. Subthreshold swing versus gate bias with V_{ds} stepping from 0 to 2V.

Optimization of Gate Oxide Thickness

The derivation and simulation of total drain current from the previous sections reveal that both the magnitude of the parallel electric fields and the integration of tunneling current in the direction perpendicular to the Si/SiO_2 interface are strongly dependent on t_{ox}. It is therefore important to characterize t_{ox} in order to achieve optimum drain current for the device. Figure 18 provides a comparison of maximum electric fields and tunneling currents at different t_{ox} for the SSSD devices, and the transistor characteristics for an SSSD device with t_{ox}=30Å are illustrated in Fig. 19. Because of the Schottky barrier at drain, SSSD devices exhibit sufficiently small I_{OFF}, until the drain barrier is overcome by biasing. Although higher electric fields result in higher current densities at smaller t_{ox} at ON state, it becomes more difficult to turn off the SSOD devices, because a very small barrier is easily overcome by the high speed electrons entering the channel. There exists at V_{ds} = 0 a noticeable amount of current increase when t_{ox} is decreased to 30Å.

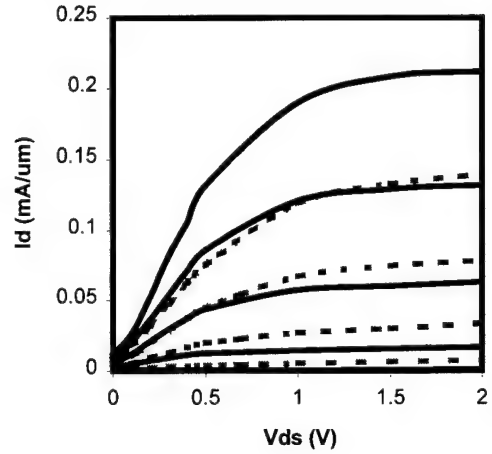


Figure 18. Calculated transistor characteristics of an SSSD MOSFET with SiGe parameters for t_{ox}=50Å (dotted lines) and 30Å (solid lines). $t_{id} = t_{ox}$.

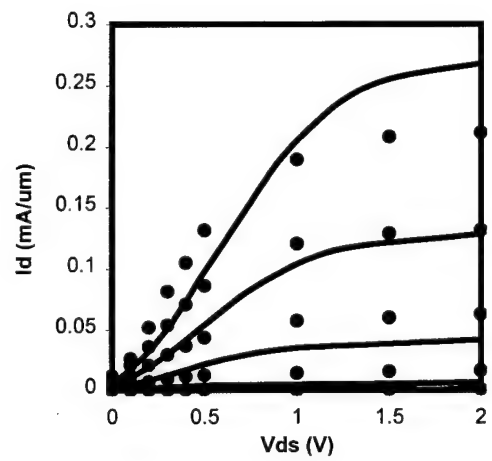


Figure 19. Simulated (solid lines) and calculated (dotted lines) transistor characteristics of an SSSD MOSFET with V_{gs} stepping evenly from 0 to 2V. t_{ox}=30Å.

VI. Conclusion

We have presented a small transistor design utilizing Schottky tunneling mechanism. The simple analytical current expression is derived from the tunneling theory. Simulations and discussion of transistor behavior are performed to verify and modify the current expression.

The drain current due to tunneling at the Schottky barrier source-channel interface is estimated by

$$I_{tSCH} \approx \frac{KQ_{SCH}E_g}{6P_{SCH}}\xi_0^2 \exp\left(-\frac{P_{SCH}}{\xi_0}\right)\cdot t_{id}$$

where P_{SCH} and Q_{SCH} are tunneling constants, ξ_0 the maximum corner electric field, and t_{id} the integration distance along the direction perpendicular to the Si/SiO_2 interface.

The drain current is in the 0.2mA/μm range when the transistor enters saturation mode. Gate capacitance is also reduced comparing to a conventional MOSFET; therefore, the cutoff frequency can reach approximately 150GHz. With Ohmic drain (SSOD devices), the saturation voltage $V_{ds,SAT}$ of the device is approximately equal to the difference between the metal Fermi level and the valance band edge of the semiconductor at the metal-semiconductor interface (~0.5V). However, with Schottky drain (SSSD devices), the Schottky barrier height also contributes as an additional term in $V_{ds,SAT}$ (~1V). The tunneling parameters in this analysis are extracted from Al-SiGe. Current fabrication technology provides possible tuning of Schottky barrier height to semiconductor by employment of silicided material. By lowering the barrier height, Schottky tunneling current can be further enhanced.

The characterization of V_T is also advantageous in the tunneling device. As subthreshold current is dominated by thermionic tunneling, V_T is determined by Schottky barrier height and flatband voltage, and independent of device doping. Since t_{ox} is required for high electric field only at the corner, its thickness over the entire channel is not critical for high transconductance. Current fabrication technology suggests a step-oxide possibility. The critical thickness is only necessary for a small area covering the source corner (Fig. 20). Because lower electric fields result from larger t_{ox} at the drain edge, simulation shows that the device exhibits a better saturation characteristic: flatter IV curves at an earlier V_{gs}. This offers another superb advantage in utilizing Schottky tunneling mechanism in this structure.

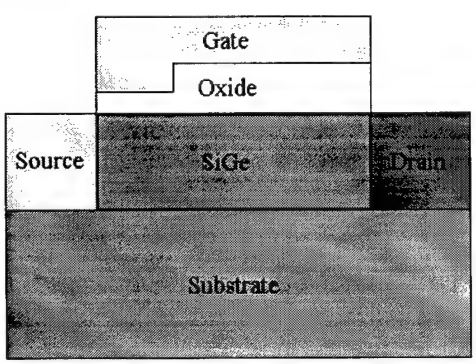


Figure 20. Schematic structure of a Schottky source MOSFET similar to Fig. 1, except gate oxide thickness is thinner near the corner of source-channel- front Si/SiO_2 interface.

VII. Appendix

Schottky Tunneling Current Density

The tunneling probability is of the form

$$T_t \approx \exp\left(\frac{-4\sqrt{2}m^{*1/2}E_g^{3/2}}{3q\hbar\xi}\right)\exp\left(\frac{-2E_\perp}{\overline{E}}\right)$$

where m^* is the effective mass, E_g the bandgap of the semiconductor and ξ the electric field. $\overline{E}$, the measure of the significant range of transverse momentum, is given by

$$\overline{E} = \frac{4\sqrt{2}q\hbar\xi}{3\pi m^{*1/2}E_g^{1/2}}$$

The induced current per unit area in the energy range $dE_x dE_\perp$ is given by

$$dJ_x = \frac{qm^*}{2\pi^2\hbar^3}dE_x dE_\perp$$

where E_x is the energy associated with momentum in the tunneling direction. The tunneling current per unit area can be obtained with the above equations,

$$J_t = \frac{qm^*}{2\pi^2\hbar^3}\int_0^\infty T_t\left(F_c(E)-F_v(E)\right)dEdE_\perp$$

where $F_c(E)$ and $F_v(E)$ are the occupancy factors. Since the device is reverse biased, $F_c(E) = 0$, and $F_v(E) = 1$. The integral becomes

$$J_{tSCH} = \frac{K}{2}\int_0^{E_g-q\phi_{sb}} \exp\left(\frac{-A_{SCH}}{\xi_0}\right)B_{SCH}\xi_0 dE_x$$

where tunneling parameters A_{SCH}, B_{SCH}, and K are given by

$$A_{SCH} = \frac{4\sqrt{2}m^{*1/2}\left(q\phi_{sb}+E_x\right)^{3/2}}{3q\hbar}$$

$$B_{SCH} = \frac{4\sqrt{2}q\hbar}{3\pi m^{*1/2}\left(q\phi_{sb}+E_x\right)^{1/2}},$$

$$K = \frac{qm^*}{2\pi^2\hbar^3}.$$

Material parameters in these tunneling constants are separated from the varying term E_x, grouped and defined as

$$P_{SCH} = \frac{4\sqrt{2}m^{*1/2}(q\phi_{sb})^{3/2}}{3q\hbar},\quad Q_{SCH} = \frac{4\sqrt{2}q\hbar}{3\pi m^{*1/2}(q\phi_{sb})^{1/2}},$$

The incident current density is re-written as

$$J_{tSCH} = \frac{K}{2} \int_0^{(E_g - q\phi_{sb})} \exp\left(\frac{-P_{SCH}}{\xi_0} \left(1 + \frac{E_x}{q\phi_{sb}}\right)^{3/2} \right) \frac{Q_{SCH}\xi_0}{\left(1 + \frac{E_x}{q\phi_{sb}}\right)^{1/2}} dE_x$$

where ϕ_{sb} is the Schottky barrier height. A close form expression is provided as

$$J_{tSCH} = \frac{KQ_{SCH}}{18P_{SCH}^{\ 2}} \xi_0^2 \exp\left(-\frac{P_{SCH}}{\xi_0}\right) \left(\exp\left(-\frac{3P_{SCH}\left(E_g - q\phi_{sb}\right)}{2\xi_0 q\phi_{sb}} \right) \left(-6q\phi_{sb}P_{SCH} + 3P_{SCH}\left(E_g - q\phi_{sb}\right) + 2q\phi_{sb}\xi_0 \right) - 2q\phi_{sb}\left(-3P_{SCH} + \xi_0\right) \right)$$

For Si- or SiGe-Al interfaces, Schottky barrier height is roughly ⅔ of the semiconductor bandgap. We can further simplify the expression of J_{tSCH} as

$$J_{tSCH} = \frac{KQ_{SCH}}{2} \xi_0^2 \exp\left(-\frac{P_{SCH}}{\xi_0}\right) C_{corr}$$

where the correction factor C_{corr} represents barrier heights and bandgap parameters:

$$C_{corr} = \frac{E_g}{9P_{SCH}^{\ 2}} \left(\exp\left(\frac{-3P_{SCH}}{4\xi_0}\right) \left(-3P_{SCH} + \frac{4\xi_0}{3}\right) + \left(4P_{SCH} - \frac{4\xi_0}{3}\right) \right)$$

$$C_{corr} \approx \frac{E_g}{9P_{SCH}^{\ 2}} \left(4P_{SCH} - \frac{4\xi_0}{3}\right)$$

Since $\left(4P_{SCH} >> \frac{4\xi_0}{3}\right)$, C_{corr} is further approximated, and the current density expression is

$$J_{tSCH} \approx \frac{KQ_{SCH}E_g}{6P_{SCH}} \xi_0^2 \exp\left(-\frac{P_{SCH}}{\xi_0}\right)$$

Derivation of Parallel Electric Field

The derivative of potential distribution with respect to the position in the tunneling direction, yields the parallel electric field expression:

$$\xi_{xf}(x) = \frac{\alpha_f^{\ 1/2}}{1 - \exp\left(-2\Gamma_f\right)} \left\{ \left(\sigma_f - \left(\sigma_f + V_{ds}'\right)\exp\left(-\Gamma_f\right)\right)\exp\left(-\alpha_f^{\ 1/2}x\right) - \left(\left(\sigma_f + V_{ds}'\right) - \sigma_f \exp\left(-\Gamma_f\right)\right)\exp\left(-\alpha_f^{\ 1/2}(L - x)\right) \right\}$$

where

$$\alpha_f = \frac{2\left(1 + \frac{\varepsilon_{ox}t_{si}}{\varepsilon_{si}t_{ox}} + \frac{\varepsilon_{ox}t_{box}}{\varepsilon_{ox}t_{ox}}\right)}{t_{Si}^2\left(1 + 2\frac{\varepsilon_{si}t_{box}}{\varepsilon_{ox}t_{si}}\right)}$$

$$\Gamma_f = L \cdot \alpha_f^{\ 1/2}$$

$$\sigma_f \approx -V_{gs}'$$

$$V_{ds}' \approx V_{ds} + \phi_{sb} - \phi_{bi}$$

At the metal-semiconductor interface ($x = 0$),

$$\xi_{xf} \approx \alpha_f^{\ 1/2} \left(\sigma_f \frac{1 - \exp\left(-\Gamma_f\right)}{1 + \exp\left(-\Gamma_f\right)} - 2V_{ds}' \frac{\exp\left(-\Gamma_f\right)}{1 - \exp\left(-2\Gamma_f\right)} \right)$$

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Theory of Generalized Drift-Diffusion Model

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Abstract

By taking the appropriate moments of the Boltzmann transport equation, we show that the mobility and diffusion constants can be rigorously defined for the most general nonstationary transport condition, including the velocity overshoot and the ballistic case. The moments are obtained by using a special parameter called Asymmetric Relaxation Time. The theory can provide a fundamental basis for constructing compact circuit models for all deep submicron devices and sub 100nm devices. It can also be used to construct efficient models for device TCAD simulators.

I. Introduction

The Boltzmann Transport Equation (BTE) provides the foundation of modeling carrier transport in modern devices and the devices of near future. The conventional drift-diffusion (DD)model for carrier transport is the first moment of the BTE. [1] As the minimum feature sizes of the devices came to the submicron regime, it became necessary to include higher order of moments of the BTE to account for the nonstationary effects. The resultant set of equations are usually referred to as the hydrodynamic equations (HD)M [2]. Today, most of the existing device simulators incorporate some extent of a HD model. The differences among the various HD models are due to different ways of modeling the carrier distribution function, the carrier energy band structure, and the microscopic relaxation times of the collision term [2]. Of course, the Monte Carlo (MC) method is the most accurate solution of the BTE [3]. It is still considered to be too uneconomical to be directly used for semiconductor device design.

Even though the HD model is more efficient than the MC method, it is still much more time consuming than the DD model. As a engineering design tool, both the accuracy and economy of the model are extremely important. To meet the trend of a shortened development cycle and more stringent performance demand, the semiconductor industry has an immediate need in accurate physics based device simulators with fast computation turn-around time. There are many reasons that a new approach should be sought. We have endeavored an investigation in this direction and found that a generalized drift-diffusion (GDD) model can be developed rigorously based on BTE. The GDD approach can be very accurate since the two basic parameters, generalized mobility and diffusivity, are precisely defined. We then need to model these parameters. Once they are properly modeled, the simulation time will be similar to the conventional DD model which is known to be very efficient.

II. Theory

The Boltzmann Transport Equation is given by

$$\frac{\partial f(\vec{r},\vec{k},t)}{\partial t} = -\vec{v}\cdot\nabla_{\vec{r}} f(\vec{r},\vec{k},t) - \frac{\vec{E}}{\hbar}\cdot\nabla_{\vec{k}} f(\vec{r},\vec{k},t) + \left(\frac{\partial f}{\partial t}\right)_{coll} \qquad (1)$$

For the analysis of very small devices, $(\frac{\partial f}{\partial t}) \cong 0$. The distribution function is determined by three terms. The term with $\nabla_{\vec{r}}$ corresponds to diffusion motion, the term with $\nabla_{\vec{k}}$ corresponds to drift motion and the last term represents the effect of collisions. For non-degenerate carriers,

$$(\frac{\partial f}{\partial t})_{coll} = \int d\vec{k}' \left[f(\vec{k}',\vec{r},t) \cdot S(\vec{k}',\vec{k}) - f(\vec{k},\vec{r},t) \cdot S(\vec{k},\vec{k}') \right] \qquad (2)$$

To make the most general interpretation of drift and diffusion, we will define a relaxation time called Asymmetric Relaxation Time (ART). The ART will be the momentum relaxation time (MRT) when the latter exist. Note that the existence of momentum relaxation time gives a most simple but rigorous description of the drift-diffusion model. When scattering mechanisms are velocity randomizing or quasi-elastic, the momentum relaxation time exists [4]. In silicon these conditions are satisfied in an approximate sense. But for scattering mechanisms such as the polar optical phonon scattering in GaAs, the conditions are not satisfied. The ART can play the same role as MRT.

From the BTE, it is natural to divide the current density into two parts even in the most general case. As shown, the time independent BTE has three terms: diffusion, drift and collision. If we can take an appropriate moment of the collision term to make it a current density, we then can obtain a general drift and diffusion model. Of course, in order to be useful, the chosen form of the moment should be simple and have clear physical meaning. It turns out such a form is indeed possible. We find that we can divide the distribution function into symmetric and asymmetric parts. Due to time reversal symmetry, the collision matrix elements have some very general properties. It can be shown that these properties will maintain the symmetry and asymmetry of the distribution function. Only the asymmetric part of the distribution provides the current. We can use the relaxation time ART for the asymmetric distribution to define the required form of the moment. As will be shown in the following, the symmetric part of the distribution makes zero contribution to the moment due to time reversal symmetry. The collision term then produces the current density and the other two terms generate the precise definitions of the generalized drift and diffusion current. The ART is similar to the MRT in physical meaning but is much more general. It encompasses all the transport conditions that BTE can describe,

including the nonstationary transport and nearly ballistic case. A more detailed account is provided in the following.

To define ART, separate f into symmetric and asymmetric parts

$$f(\vec{r},\vec{k},t) \;=\; f_0(\vec{r},\vec{k},t) \;+\; f_1(\vec{r},\vec{k},t) \tag{3a}$$

$$f_0(\vec{r},\vec{k},t) \;=\; \frac{f(\vec{r},\vec{k},t)+f(\vec{r},-\vec{k},t)}{2} \tag{3b}$$

$$f_1(\vec{r},\vec{k},t) \;=\; \frac{f(\vec{r},\vec{k},t)-f(\vec{r},-\vec{k},t)}{2} \tag{3c}$$

Therefore,

$$\left(\frac{\partial f}{\partial t}\right)_{coll} \;=\; \left(\frac{\partial f_0}{\partial t}\right)_{coll} \;+\; \left(\frac{\partial f_1}{\partial t}\right)_{coll} \tag{4a}$$

Define $$\left(\frac{\partial f_1}{\partial t}\right)_{coll} \;\equiv\; \frac{-f_1(\vec{r},\vec{k},t)}{\tau(\vec{r},\vec{k},t)}, \tag{4b}$$

where the relaxation time $\tau(\vec{r},\vec{k},t)$ is called ART because it describes the collision effects on the asymmetric part of the distribution function. It can be shown that this relaxation time alone determines the local current density. Take the momentum of

$$\vec{Q}(\vec{r},\vec{k},t) \;\equiv\; -\; e\vec{v}(\vec{k})\tau(\vec{r},\vec{k},t) \quad . \tag{5}$$

Then, we have

$$-\;\vec{Q}(\vec{v}\cdot\nabla_{\vec{r}}f) \;-\; \vec{Q}\left(\frac{e\vec{F}}{\hbar}\cdot\nabla_{\vec{k}}f\right) \;+\; \vec{Q}\left(\frac{\partial f_1}{\partial t}\right)_{coll} \;+\; \vec{Q}\left(\frac{\partial f_0}{\partial t}\right)_{coll} \;=\; 0 \tag{6a}$$

$$\left\langle \vec{Q}\left(\frac{\partial f_1}{\partial t}\right)_{coll}\right\rangle \;=\; -\;e\int \vec{v}(\vec{k})f_1(\vec{r},\vec{k},t)\frac{d\vec{k}}{4\pi^3} \;=\; \vec{J}(\vec{r},t) \tag{6b}$$

$$\left\langle \vec{Q}\left(\frac{\partial f_0}{\partial t}\right)_{coll}\right\rangle \;=\; -\;e\int \vec{v}(\vec{k})\tau(\vec{r},\vec{k},t)\left(\frac{\partial f_0(\vec{r},\vec{k},t)}{\partial t}\right)_{coll}\frac{d\vec{k}}{4\pi^3} \tag{6c}$$

It can be shown in Appendix A that

$$\tau(\vec{r},\vec{k},t) \;=\; \tau(\vec{r},-\vec{k},t), \tag{7a}$$

$$\left(\frac{\partial f_0(\vec{r},\vec{k},t)}{\partial t}\right)_{coll} \;=\; \left(\frac{\partial f_0(\vec{r},-\vec{k},t)}{\partial t}\right)_{coll} \tag{7b}$$

From Eq.(7a) and (7b), it can be shown that

$$\langle \vec{Q}(\frac{\partial f_0}{\partial t})_{coll} \rangle \;=\; 0\,. \tag{8}$$

We can neglect the $\vec{r}$ dependence of $\tau(\vec{r},\vec{k},t)$ when compared with $f(\vec{r},\vec{k},t)$ (which changes much faster than τ).Then, the diffusion term can be written as

$$-e\int \vec{v}(\vec{k})\tau(\vec{r},\vec{k},t)(\vec{v}\cdot\nabla_{\vec{r}} f(\vec{r},\vec{k},t))\frac{d\vec{k}}{4\pi^3} = \;-\; e\;\nabla_{\vec{r}}\int \tau v_{\hat{F}}^2 f(\vec{r},\vec{k},t)\frac{d\vec{k}}{4\pi^3} \tag{9}$$

We assume that f changes in the direction of the electric field, the diffusion current deisity can be defined as (if not, it can be easily generalized as a tensor)

$$J_{diffusion} \equiv \;-\; e\;\nabla_{\vec{r}} D(\vec{r},t)\cdot n(\vec{r},t) \quad . \tag{10a}$$

Then, the generalized diffusivity is given by,

$$D(\vec{r},t) \;\equiv\; \frac{\int \tau(\vec{r},\vec{k},t) v_{\hat{F}}^2 f(\vec{r},\vec{k},t)\frac{d\vec{k}}{4\pi^3}}{\int f(\vec{r},\vec{k},t)\frac{d\vec{k}}{4\pi^3}} \;=\; \frac{\int \tau(\vec{r},\vec{k},t) v_F^2 f_0(\vec{r},\vec{k},t)\frac{d\vec{k}}{4\pi^3}}{\int f_0(\vec{r},\vec{k},t)\frac{d\vec{k}}{4\pi^3}} \tag{10b}$$

Similarly, drift term can be used to define a generalized mobility

$$-\;e\;\int \vec{v}(\vec{k})\tau(\vec{r},\vec{k},t)\left(\frac{\vec{E}}{n}\cdot\nabla_{\vec{k}} f(\vec{r},\vec{k},t)\right)\frac{d\vec{k}}{4\pi^3} \equiv \;+\; en\mu(\vec{r},\vec{E},t)\vec{E}(\vec{r},t) \quad , \tag{11a}$$

with

$$\mu(\vec{r},t) \;=\; \frac{-\int (v_{\hat{E}}(\vec{k}))\tau(\vec{r},\vec{k},t)\frac{\partial}{\partial k_{\hat{E}}} f(\vec{r},\vec{k},t)\frac{d\vec{k}}{4\pi^3}}{\int f(\vec{r},\vec{k},t)\frac{d\vec{k}}{4\pi^3}} \quad . \tag{11b}$$

The generalized diffusivity and mobility defined in Eqs.(10b) and (11b) applies to any situation of nonstationary transport, including the limiting case of nearly ballistic transport.

III. Simple Cases

Some simplified expression can be derived if the distribution function can be simplified. In the following, it is shown for the case that a single hot electron temperature can be used to characterize the distribution function.

When $f(\vec{r},\vec{k},t) = e^{(E_F-E)/kT_c}$, it can be shown that

$$\mu(\vec{r},t) = \frac{\frac{e}{kT_c}\int v_E^2 \tau(\vec{r},\vec{k},t) f_0 \frac{d\vec{k}}{4\pi^3}}{\int f_0 \frac{d\vec{k}}{4\pi^3}} = \frac{e}{kT_c} D(\vec{r},t), \tag{12}$$

where T_c is the hot electron temperature.

For a more general case that a single hot electron temperature can not be used to characterize the distribution but the asymmetric part of the distribution can be neglected in the generalized mobility, then

$$\mu(\vec{r},t) = \frac{-\int v_E(\vec{k})\tau(\vec{r},\vec{k},t)\hat{E}\cdot\nabla_{\vec{k}} f_0(\vec{r},\vec{k},t)\frac{d\vec{k}}{4\pi^3}}{\int f_0(\vec{r},\vec{k},t)\frac{d\vec{k}}{4\pi^3}} \tag{13}$$

If $\hat{E}\cdot\nabla_{\vec{k}} f_0(\vec{r},\vec{k},t) = \frac{\partial f_0}{\partial E}\hbar\vec{v}_E$,

$$\mu(\vec{r},t) = \frac{e\int \tau v_E^2 (-\frac{\partial}{\partial E}\ln f_0)\cdot f_0(\vec{r},\vec{k},t)\frac{d\vec{k}}{4\pi^3}}{\int f_0(\vec{r},\vec{k},t)\frac{d\vec{k}}{4\pi^3}} \tag{14}$$

The generalized Einstein relationship becomes,

$$\mu \equiv \frac{e}{kT_c} D \tag{15}$$

The carrier temperature for Einstein relation is given by,

$$\frac{1}{kT_c} \equiv \frac{\int (-\frac{\partial}{\partial E}\ln f_0)\tau v_E^2 f_0(\vec{r},\vec{k},t)\frac{d\vec{k}}{4\pi^3}}{\int \tau v_E^2 f_0(\vec{r},\vec{k},t)\frac{d\vec{k}}{4\pi^3}} \tag{16}$$

If the band is isotropic,

$$\tau v_E^2 = \frac{1}{3}\tau v^2 \text{ and}$$

$$\frac{1}{kT_c} = \frac{\int_0^\infty \left(-\frac{\partial}{\partial E}\ln f_0\right)\tau v^2 f_0 D(E)dE}{\int \tau v^2 f_0 D(E)dE} \qquad (17)$$

In Eq.(17), the hot carrier temperature for generalized Einstein relation is given by the local energy temperature $-\frac{\partial}{\partial E}\ln f_0$ weighted by the product $\tau(E)v(E)^2 f_0(E)D(E)$.

IV. Discussion

There are many good reasons why this approach should be very useful.

1 The TCAD field is becoming a mature industry. The time to industry availability of new physical models is shrinking from years to days. This important trend encourages the development of modules of device-specific models. An outstanding example is the ultra-fast device simulation with MC tuned transport models in FastBlaze. The speed is greatly enhanced while accuracy is the same or even improved. With the GDD model, the speed will be further improved when compared with the energy balance simulation. The accuracy can also be improved because the GDD parameters are precisely defined while the energy balance parameters are approximately defined. Of course, the GDD parameters can be MC tuned.

1. As the minimum feature sizes of the devices are moving into the sub-100nm regime, nearly ballistic types of motion may appear in a substantial part of the active device region. Therefore, more and more higher order moments of BTE are required to ensure accuracy. This can be easily expected since a nearly ballistic distribution function requires many moments to represent it. The required simulation time will then increase greatly. As will be shown later, the GDD parameters are precisely defined in terms of the local distribution function. It takes care of nearly ballistic electrons as easy (in some sense easier) as the thermalized hot electrons.

2. As more hetorojunctions are used in special devices, the tunneling current may affect the mobility and diffusivity in the future devices. The HD model will be again very tedious in dealing with these effects. For the GDD model, it is natural to treat these effects as in the nearly ballistic type of transport.

4 As the Semiconductors Roadmap [6] has emphasized, timely access to accurate computer models of each technology area will be necessary to managing the growing complexity of the semiconductor technology. Different levels of abstraction for models are essential to effectively shorten time scales, lower cost, and increase quality. In device TCAD area, how to build compact circuit models for device is as important as the device simulation. In doing this, effective parameter extraction for device simulation results are of increasing importance. Since most analytical works for device modeling have been done in terms of drift–diffusion model, the usage of GDD will naturally make the task of compact circuit modeling much easier than the HD or MC approach. For example, there is up until now no rigorous Gummel-Poon type model for HBT since the nonstationary transport involved here cannot be put into simple analytical forms. Using GDD approach, it will be straightforward to set up such compact circuit models.

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Appendix A: Proof

Note: in the following , we present the proof of

(1) $\tau(\vec{r},\vec{k},t) = \tau(\vec{r},-\vec{k},t)$

(2) $\left.\frac{\partial f_0(\vec{r},\vec{k},t)}{\partial t}\right|_{coll} = \left.\frac{\partial f_0(\vec{r},-\vec{k},t)}{\partial t}\right|_{coll}$

To prove (1), let

$$\frac{1}{\tau(\vec{r},\vec{k},t)} = \int \frac{d\vec{k}'}{8\pi^3} S(\vec{k},\vec{k}') - \frac{1}{f_1(\vec{r},\vec{k},t)} \int \frac{d\vec{k}'}{8\pi^3} f_1(\vec{r},\vec{k}',t)\cdot S(\vec{k}',\vec{k})$$

$$\frac{1}{\tau(\vec{r},\vec{k},t)} = \int \frac{d\vec{k}'}{8\pi^3} S(\vec{k},\vec{k}') - \frac{1}{f(\vec{r},\vec{k},t)-f(\vec{r},-\vec{k},t)} \int \frac{d\vec{k}'}{8\pi^3} \left[f(\vec{r},\vec{k}',t) - f(\vec{r},-\vec{k}',t) \right] S(\vec{k}',\vec{k})$$

$$\frac{1}{\tau(\vec{r},-\vec{k},t)} = \int \frac{d\vec{k}'}{8\pi^3} S(-\vec{k},\vec{k}') - \frac{1}{f(\vec{r},-\vec{k},t)-f(\vec{r},\vec{k},t)} \int \frac{d\vec{k}'}{8\pi^3} \left[f(\vec{r},\vec{k}',t) - f(\vec{r},-\vec{k}',t) \right] S(\vec{k}',-\vec{k})$$

By time reversal symmetry [5]

$$S(\vec{k},\vec{k}') = S(-\vec{k},-\vec{k}')$$

$$S(-\vec{k},\vec{k}') = S(\vec{k},-\vec{k}')$$

$$\frac{1}{\tau(\vec{r},-\vec{k},t)} = \int \frac{d\vec{k}'}{8\pi^3} S(\vec{k},-\vec{k}') - \frac{1}{f(\vec{r},-\vec{k},t)-f(\vec{r},\vec{k},t)} \int \frac{d\vec{k}'}{8\pi^3} \left[f(\vec{r},\vec{k}',t) - f(\vec{r},-\vec{k}',t) \right] S(-\vec{k}',\vec{k})$$

$$= \int \frac{d\vec{k}''}{8\pi^3} S(\vec{k},\vec{k}'') - \frac{(-1)}{f(\vec{r},\vec{k},t)-f(\vec{r},-\vec{k},t)} \int \frac{d\vec{k}''}{8\pi^3} \left[f(\vec{r},-\vec{k}'',t) - f(\vec{r},\vec{k}'',t) \right] S(\vec{k}'',\vec{k}) = \frac{1}{\tau(\vec{r},\vec{k},t)}$$

This is reasonable, because only when $\tau(\vec{r},\vec{k},t) = \tau(\vec{r},-\vec{k},t)$, the asymmetry of $f_1(\vec{r},\vec{k},t)$ can be maintained.

To prove (2)

(2) $$\left(\frac{\partial f_0(\vec{r},\vec{k},t)}{\partial t} \right)_{coll} = \int \frac{d\vec{k}'}{8\pi^3} \left[f_0(\vec{r},\vec{k}',t) \cdot S(\vec{k}',\vec{k}) - f_0(\vec{r},\vec{k},t) \cdot S(\vec{k},\vec{k}') \right]$$

$$\left(\frac{\partial f_0(\vec{r},-\vec{k},t)}{\partial t} \right)_{coll} = \int \frac{d\vec{k}'}{8\pi^3} \left[f_0(\vec{r},\vec{k}',t) \cdot S(\vec{k}',-\vec{k}) - f_0(\vec{r},-\vec{k},t) \cdot S(-\vec{k},\vec{k}') \right]$$

$$S(\vec{k}',-\vec{k}) = S(-\vec{k}',\vec{k}) \qquad \text{(time reversal)}$$

$$= \int \frac{d\vec{k}'}{8\pi^3} \left[f_0(\vec{r},\vec{k}',t) \cdot S(-\vec{k}',\vec{k}) - f_0(\vec{r},-\vec{k},t) \cdot S(\vec{k},-\vec{k}') \right]$$

$$= \int \frac{d\vec{k}''}{8\pi^3} \left[f_0(\vec{r},\vec{k}'',t) \cdot S(\vec{k}'',\vec{k}) - f_0(\vec{r},\vec{k},t) \cdot S(\vec{k},\vec{k}'') \right]$$

$$= \left(\frac{\partial f_0(\vec{r},\vec{k},t)}{\partial t} \right)_{coll}$$

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150Gsample/s wavelength division sampler with time-stretched output

A.S. Bhushan, F. Coppinger, B. Jalali, S. Wang and H.F. Fetterman

A new technique for optical sampling and time stretching of an analogue signal is presented. The signal is 'wavelength stamped' by a chirped optical pulse. An arrayed waveguide grating provides parallel time-interleaved samples as well as a time-stretched serial sampled waveform.

High-speed analogue-to-digital conversion systems require sampling techniques that have high temporal resolution and fast sampling rates. Also of great importance is a mechanism for demultiplexing or slowing the samples in time as they approach the electronic quantiser. If time could be mapped onto wavelength, then the problem of demultiplexing in time could be translated into a problem of demultiplexing in wavelength. The latter can be resolved easily by using just passive optical filters. Time-to-wavelength mapping by mixing a chirped pulse with a digital data stream has been used to demultiplex digital serial data [1]. Chirping a broadband transform-limited pulse separates different spectral components of the pulse in time. When the chirped pulse enters the mixer, different wavelength components arrive sequentially. Thus, time is mapped into the optical wavelength. This technique has also been applied to transmission of WDM data [2] and to sample analogue signals [3, 4]. In this Letter, we demonstrate a novel sampling architecture based on two complimentary concepts. The first is the chirped-pulse time-to-wavelength transformation. The second is the use of discrete dispersion, obtainable with an arrayed waveguide grating (AWG) [5], to slow down the sampled waveform.

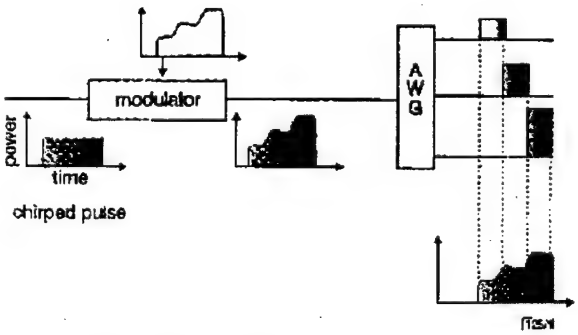

Fig. 1 *Wavelength division sampling*

Different shades of grey represent different wavelengths

The chirped pulse sampling is shown in Fig. 1. To generate chirped pulses, we use a passively modelocked erbium-doped fibre dispersion in a singlemode fibre (SMF, D = 17ps/nm.km). Sampling is performed by a silica AWG with a channel spacing of 0.8nm and a passband of 0.3nm. The electrical signal and the chirped pulse interact in the optical modulator to produce a 'wavelength stamped' intensity-modulated optical signal. The AWG samples the optical spectrum and thus samples the time evolution of the electrical transient. In Fig. 2, we report the timing measurements for a chirp of 120ps/nm (7km of SMF). Outputs from individual AWG ports are photodetected and displayed using a digital-sampling oscilloscope. The pulse-to-pulse spacing of 100ps in Fig. 2 corresponds well to the channel spacing of 0.8nm for the AWG.

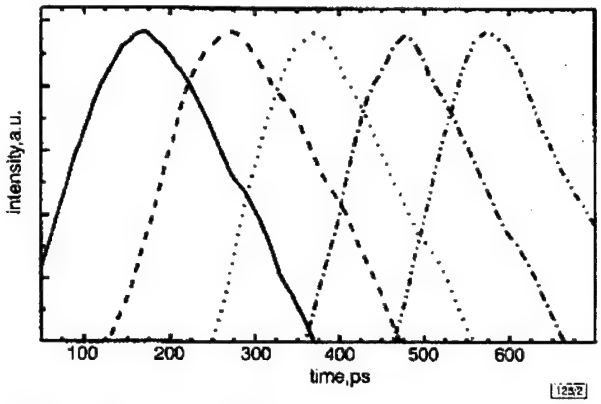

Fig. 2 *Timing measurements at 10Gsample/s*

Each trace is a different output of the AWG

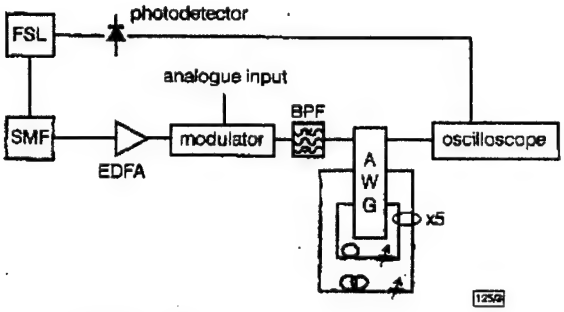

Fig. 3 *Experimental setup*

FSL denotes femtosecond laser

The setup for the 150Gsample/s experiment is shown in Fig. 3. The transform-limited pulse from the EDFL was dispersed through a Corning SMF to produce a chirped pulse. A portion of the femto-second laser output is fed to a photodetector to provide the synchronising clock for the entire system. The chirped pulse is modulated and then fed to an 8-channel silica AWG. A 5nm bandpass filter precedes the AWG so that the serialised output contains only one free spectral range of the AWG. The outputs of the AWG are fed back to the corresponding inputs with incremental delays of around 1.3ns. This feedback architecture provides discrete dispersion and separates samples in time. In an analogue-to-digital (A/D) converter system, a single slow electronic quantiser can then be used to digitise a fast electrical transient. The feedback paths include variable attenuators to provide spectral equalisation. Spectral equalisation can also be attained by using a dispersion-decreasing super-continuum fibre [6] or by a feed forward architecture [2]. The sampling rate is given by $f_s = 1/\Delta\lambda . D$, where $\Delta\lambda$ is the AWG channel spacing and D is the total dispersion. We use a 500m spool of fibre for dispersion corresponding to a chirp rate of 8.5ps/nm at the modulator input. The pulse separation (in time) at the output of each AWG channel is 6.8ps, corresponding to a sampling rate of 147Gsample/s. The response time of the photodetector (30ps) and the jitter noise in the measuring electronics (1.3ps) make measuring the actual pulse-to-pulse separation difficult. However, the separation between the first and the last channel outputs (before feedback) was measured to be 32ps, which corresponds to an average pulse separation of 6.4ps. Fig. 4 shows the time-stretched serialised output. The output rate is reduced from 147GHz to 770MHz by 1.3ns incremental delays in

half-to-noise ratio (SNR) reflected in the nonuniformity in the sample stream is 14dB. In general, the SNR has a contribution from the spectral nonuniformity (from laser and AWG) as well as crosstalk within the AWG. Since the measured AWG optical crosstalk is 27dB, we conclude that the measured SNR is limited by the incomplete spectral equalisation, which can be improved with higher quality attenuators.

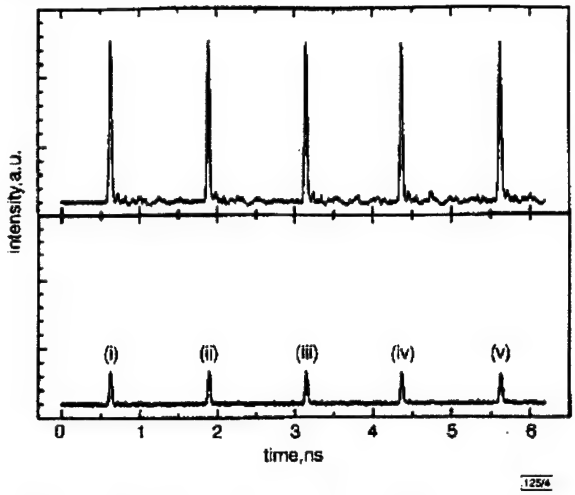

Fig. 4 *Time stretched and serialised output for 147Gsample/s sampling*

Modulator voltage = 1V (top trace) and 8V (bottom trace)
$V\pi$ = 10V
(i) λ = 1565.4nm
(ii) λ = 1566.2nm
(iii) λ = 1567nm
(iv) λ = 1567.8nm
(v) λ = 1568.6nm

In summary, we have demonstrated a novel optical sampling method. The chirped pulse technique provides time-interleaved samples compatible with interleaved A/D architecture. Using an AWG in a recirculating configuration, a stream of samples can be stretched in time and serialised, allowing an ultra-fast electrical transient to be digitised with a single slow A/D.

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compensation

M. Suzuki, I. Morita, K. Tanaka, N. Edagawa, S. Yamamoto and S. Akiba

160Gbit/s (8 × 20 Gbit/s) soliton WDM signals were successfully transmitted over 4000km with a BER of < 10^{-9}, by using periodically dispersion-compensated dispersion-flattened fibre with an average dispersion slope of 0.0005ps/km/nm².

Soliton-WDM transmission is attractive for large-capacity long-haul optical transmission systems because soliton-based systems have the potential to carry higher bit rate signals than NRZ systems. The key technological issues in soliton WDM transmission are the reduction of collision-induced timing jitter, four-wave mixing [1] and the dispersion slope of the transmission fibre [2]. The first two requirements can be achieved using dispersion tapered fibre spans with soliton control techniques [3, 4]. To overcome the impact of the dispersion slope, the use of dispersion-flattened fibre seems quite attractive and practical compared with a channel-by-channel dispersion compensation scheme [2, 4]. So far, we have made a preliminary report on the effectiveness of the soliton WDM systems using dispersion-flattened transmission fibre and 80Gbit/s (4 × 20Gbit/s) signals [5]. In this Letter, we show the experimental results on 160Gbit/s (8 × 20 Gbit/s) soliton WDM transmission over 4000km using dispersion-flattened fibre with periodic dispersion compensation with a wavelength bandwidth of 11.2nm.

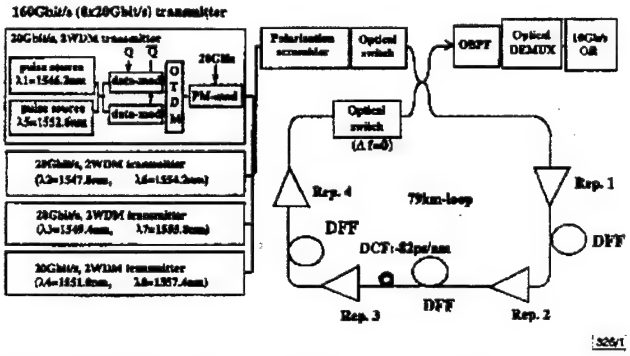

Fig. 1 *Experimental setup of 160Gbit/s (8 × 20Gbit/s) soliton WDM transmission*

Fig. 1 shows a schematic diagram of the experimental setup for eight-channel 20Gbit/s soliton WDM transmission. We used four 2WDM×20 Gbit/s transmitters as a 160Gbit/s transmitter. The wavelengths of eight channels, ranging from 1546 to 1558nm, were equally spaced by 1.6nm. Each 2WDM transmitter consists of two EA-modulator-based soliton pulse generators with different wavelengths. A 20Gbit/s optical soliton data stream was produced by using two $LiNbO_3$ intensity modulators operated at 10Gbit/s by a 2^{11} − 1 pseudorandom binary sequence and optical time division multiplexing. The pulse width obtained was from 10 to 15ps. In addition, each 20Gbit/s signal was modulated at 20GHz by an $LiNbO_3$ phase modulator to improve the transmission performance [6, 7]. After combining eight 20Gbit/s signals so that the adjacent channels were orthogonally polarised, a polarisation scrambler was used to suppress the PHB of the EDFA repeaters. The transmission line comprises three spans of ~27km long dispersion-flattened fibre (DFF) and dispersion-compensation fibre (DCF). The loss of the DFF spans, including the splicing loss, was still large and the average span loss was ~9dB. The average dispersion slope of the DFF was 0.0005ps/km/nm² and the average chromatic dispersion of the DFF at 1555nm was 1.1ps/km/nm. The accumulated chromatic dispersion of the loop was compensated for by the DCF with 82ps/nm and the residual dispersion in the loop was 0.02ps/km/nm. As a frequency guiding filter, an FP-etalon filter (*FSR* = 1.6nm) was placed in the loop to stabilise the transmission performance. In the receiver, the desired channel was selected by optical bandpass filters and the transmitted 20Gbit/s signals were optically time-division-demultiplexed to a 10Gbit/s

chirped optical pulses

F. Coppinger, A.S. Bhushan and B. Jalali

The authors report a method for stretching electrical signals in time. A high chirp rate is imposed on the electrical signal by mixing it with a dispersed ultra-short optical pulse in an electro-optic intensity modulator. This is followed by a passive optical dispersion element to produce a time-magnified copy of the input electrical signal.

Time manipulation of signals has been proposed as a possible technique to match the data rates of signals to the receiver or to observed very fast phenomena. Considering the time/space equivalence of dispersion and diffraction, and in direct analogy to a spatial lens, a signal may be stretched in time by subjecting it to a dispersion-quadratic phase modulation-dispersion sequence [1, 2]. While this concept has been known for some time, few successful experiments have been carried out due to the difficulty of obtaining high quadratic phase modulation rate and/or large bandwidth dispersive elements. In his pioneering work, Caputi demonstrated an all-electrical time stretch system [1]. In the electrical domain, highly dispersive elements are available, however the small bandwidth of these elements limits the capability and performance of an all-electrical system. Large bandwidth dispersive elements are easily obtained optically, but the dispersion remains low requiring a high quadratic phase modulation rate (or linear frequency chirping). Resonant optical phase modulators were proposed as a way to attain a high modulation rate [3]. While high chirp rates are achievable with this device, the duration of the chirp is limited. Pulses from a Nd:YAG laser were also used to create the chirp in an all-optical time lens [2]. The time aperture of the lens was then limited by the bandwidth of the pulse (620GHz). In this Letter, we demonstrate an optoelectronic time magnification system with an electrical input/output and with the linear chirp provided by a dispersed optical pulse from a modelocked erbium-doped fibre laser (EDFL). In addition to the ultra-high bandwidth (~7.5THz) and chirp rate, this system differs from previously reported time magnification systems in that the bandwidth of the input signal is negligible compared to the chirp bandwidth. With this property, an approximation to an ideal time lens can be obtained without the need to disperse the input signal. This results in a more relaxed and simpler design of a time stretching system that can readily be implemented with commercially available components. This technique is promising for analogue-to-digital conversion of ultra-fast electrical signals.

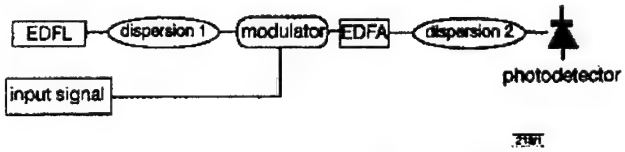

Fig. 1 *Experimental setup for time magnification using chirped optical pulse*

Fig. 1 describes our implementation of the optoelectronic time magnification system. The 160 fs pulse generated by the EDFL is dispersed in the input fibre. When the pulse reaches the modulator, different frequency components arrive at different times. The electrical signal to be stretched is efficiently mixed with the chirped optical signal by the Mach-Zehnder electro-optic modulator (12GHz bandwidth). The efficiency of the electro-optic mixing is significantly higher than optical-optical mixing [4] in a nonlinear crystal. The resulting intensity-modulated chirped signal is dispersed in a second spool of fibre and its envelope is detected by a fast photodetector with a 30ps response time.

In the experiment, we use a 2km spool of fibre to generate the frequency ramp. With a dispersion of 17ps/nm/km in the fibre, the chirp rate at the modulator is 3.5GHz/ps. To generate an arbitrary transient, we bias the modulator at V_π, and apply an electrical pulse to it. Fig. 2*a* shows the resulting waveform measured at the modulator output. It represents the applied electrical pulse, its second harmonic originating from biasing the modulator at V_π. The envelope is also somewhat shaped by the spectral envelope of the chirped pulse. The second dispersion consists of a 5.5km spool of gation through the second dispersive element. The signal is stretched in time by a factor of 3.25 with high fidelity.

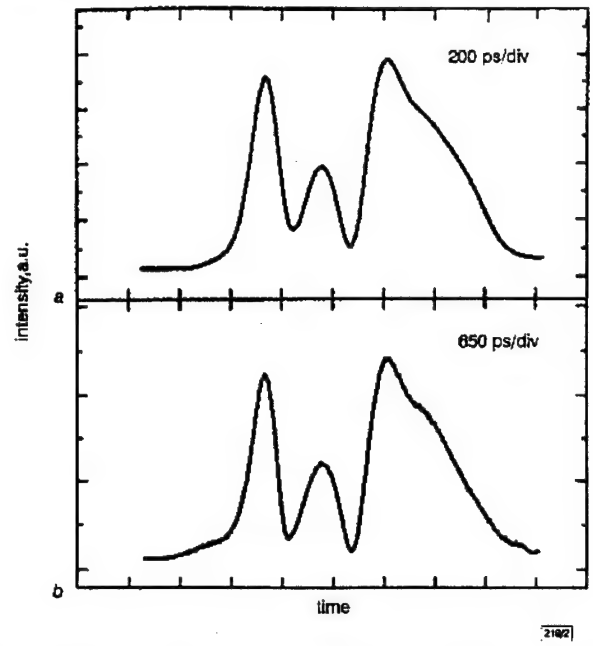

Fig. 2 *Signal envelope after modulation and magnified signal after second dispersion*

a Signal envelope after modulation
b Magnified signal after second dispersion

The magnification factor in our system depends on both the amount of dispersion in the second dispersive stage D_2 and the chirp rate. The magnification factor can be increased by increasing D_2 or by raising the chirp rate (decreasing D_1). However, increasing the chirp rate also reduces the time aperture of the system.

The fundamental resolution of a conventional time lens in which the image is at the focal time of the lens is limited by its bandwidth and is estimated to be $1/B$, where B is the chirp bandwidth [5]. If the image is not at the focal time (the case in our experiment), the image will be distorted. However, the resulting distortion is negligible as the electrical signal bandwidth (~12GHz) is negligible compared to the bandwidth of the chirp (~7.5THz). Further, the distortion is averaged out by the finite response time of the photodetector as long as $\Delta f_e D_2 < \tau_{pd}$, where Δf_e is the bandwidth of the electrical signal and τ_{pd} is the response time of the photodetector (30 ps). The resolution and linearity of the lens are also limited by the non-constant dispersion inside the fibre over the spectrum of the EDFL. Dispersion-flattened fibre would mitigate this problem. The influence of the non-flat optical spectrum on the input signal can be minimised by spectrum equalisation using a fibre Bragg grating filter, dispersion decreasing supercontinuum fibre [6], or a feedforward architecture [7].

In summary, we have used the high chirp rate offered by a dispersed pulse from an EDFL to stretch an electrical signal in time. The frequency ramp is intensity modulated by the electrical signal in a Mach-Zehnder electro-optic modulator. The chirped signal is then further dispersed leading to time magnification. This technique has potential for the digitisation of high frequency electrical signals.

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Packaged array of eight MSM photodetectors with uniform 12GHz bandwidth

R.G. DeCorby, R.I. MacDonald, A.J.P. Hnatiw, D. Boertjes, J.N. McMullin, F. Gouin and J. Noad

Transmission line concepts were used in the design of a broadband, integrated photodetector array. The array consists of eight metal semiconductor-metal (MSM) photodetectors, with active regions of $(26\mu m)^2$, distributed along a common bus. A uniform 3dB bandwidth of 12GHz is demonstrated. These arrays are central to optoelectronic switching techniques, and are applicable to microwave fibre optic systems.

Introduction: Arrays in which several photodetectors drive a single broadband load are becoming increasingly important. They were originally conceived as part of the optoelectronic switching method [1], where they are used as column vectors in the construction of a cross-point switch or signal processor [2]. Metal-semiconductor-metal (MSM) photodetectors are particularly well suited to this application [3], due to their large bandwidth, large active area, simple planar structure, and low capacitance. In addition, their symmetry allows bipolar operation and implies good on-off isolation [2]. A second emerging application of photodetector arrays is in the microwave fibre optics field, where the link insertion loss and signal-to-noise ratio may be limited by the power-handling capabilities of photodetectors in the receiver [4, 5].

We report a bandwidth of 12GHz for an integrated array of eight top-illuminated MSM detectors, packaged on a dielectric carrier with coplanar waveguide access lines. To our knowledge, this is the highest speed reported for an array of detectors with individually accessible bias lines, as required for optoelectronic switching. Previously, Liu *et al.* [6] reported 5GHz operation for an array of 4 PIN detectors.

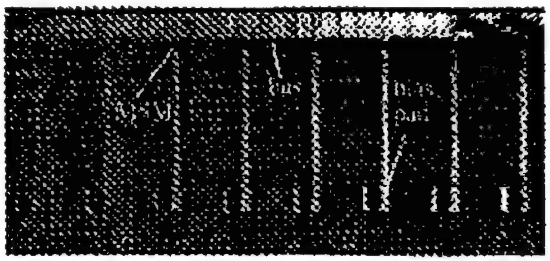

Fig. 1 *Photograph of packaged detector array*

Fabrication: Fig. 1 shows a photograph of the array reported here. Eight integrated MSM photodetectors, with $(26\mu m)^2$ active regions, are attached to a common bus, with an inter-detector spacing of 250μm. The opposite contact of each MSM provides turned on or off. The arrays were fabricated on a nominally *n*-type GaAs epitaxial layer, with a carrier concentration of $< 10^{14}cm^{-3}$. Dielectric isolation layers were omitted, but the dark current was < 100nA at an operating bias (0–10V). The interdigitated electrodes have finger spacing and a width of 2μm. After dicing, the chips were mounted on dielectric carriers with RF, coplanar-waveguide access lines. The bias pad of each MSM was wire bonded to an AC ground via a bias decoupling capacitor. The common bus was connected to the coplanar lines on the chip carrier, via multiple wire bonds at each end.

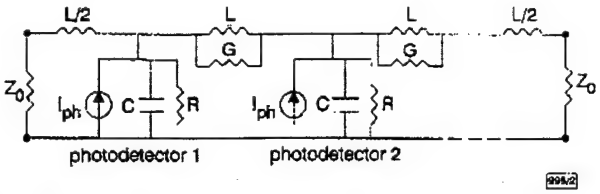

Fig. 2 *Simple equivalent circuit for array described in text*

Each end of array is terminated in system impedance

Theory: The basic theory of travelling-wave detector arrays is available elsewhere [5]. Essentially, the capacitance of a single long detector or several parallel photodetectors can be compensated by the inductance of an appropriate interconnect network, such that an artificial transmission line matched to the system impedance is formed. This is illustrated schematically in the lumped-element model of Fig. 2. The capacitance derives primarily from the photodetectors, the resistive loss terms are mainly due to finite conductivity and charge storage in the semiconductor layers, and the inductance is provided by an appropriate interconnect network, as mentioned.

At microwave frequencies, it is more accurate to treat the interconnecting lines with a distributed model. For the arrays discussed here, the interconnect network is provided by an on-wafer microstrip line, which forms the common bus. The bus is 100μm wide and 500μm from the ground plane. The impedance of this line is approximately 80Ω, and the effective propagation index is approximately 2.78. The photodetector array closely resembles a periodically loaded transmission line. The matching criteria for a terminated periodic structure are well-known, and lead to the condition [5]:

$$d_L = \frac{cZ_L C_d}{n_L\left[\frac{Z_L^2}{Z_0^2} - 1\right]} \qquad (1)$$

where d_L, Z_L, and n_L are the inter-detector length, characteristic impedance, and effective propagation index of the high-impedance interconnect, respectively. C_d is the capacitance associated with each photodetector, and Z_0 is the impedance of the external system. Eqn. 1 is valid for wavelengths greater than the period of the loaded-line structure.

The capacitance of discrete MSM photodetectors is often estimated using conformal transformation [7]. Those methods predict the capacitance associated with the interdigitated fingers only, assuming no excess charge storage in the semiconductor layers. In real MSM detectors, two other sources of parasitic capacitance must be considered. These are the capacitance associated with the bond pads and interconnect metal [7], and the so-called depletion capacitance [8] arising from charge storage deep in the semiconductor bulk or at heterojunctions. By forming these arrays on a resistive homojunction layer, grown on a semi-insulating GaAs substrate, the depletion-capacitance is minimised [7]. This simplifies the design of an impedance-matched array, since both the finger and bond-pad capacitance contributions may be predicted from layout geometry.

Experimental results: The capacitance of detectors (in the array) was determined using an on-wafer probe, and by fitting S_{22} reflection data to a simple equivalent circuit [7]. The capacitance was approximately 40–60fF, with little bias dependence. From eqn. 1, and using the high-impedance line characteristics mentioned above, the required detector capacitance for matching the array to a 50Ω system is 45fF. Assuming perfect matching (C_d = 45fF), the

A Two-Element Yagi-Uda Array Using Tunable Slot Antenna

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ABSTRACT

A two-element Yagi-Uda array with two physically equal-length slots tuned by DC bias is presented. By changing the DC bias of two reactive FET circuits imposed upon both ends of the slot, one of the two slots can be made shorter electromagnetically and serves as a director so that a two-element Yagi-Uda antenna array is achieved.

I. INTRODUCTION

Printed slot antennas fed by microstrip lines have been extensively used in radar and communication systems, mainly due to their wider bandwidth in comparison with patch antennas, low cross-polarization, as well as good isolation with the active circuitry. Recently, slot antennas integrated with active components have expanded their application even more [1]. In general, the integration of active devices provides a control mechanism for antenna performance that is not possible with passive antennas.

Traditionally, a two-element Yagi-Uda antenna array is made of two dipoles or slots with different physical lengths, in which one of the two slots is shorter or longer than the other to serve as a director or a reflector, respectively [2]. Such configuration, however, has the direction of the mainbeam fixed as the geometrical structure is decided. In [3], a slot antenna with electronically tunable length was reported. In this paper, a novel idea of utilizing two physically equal-length slot antennas in which either one slot is tunable in electrical length to achieve a Yagi-Uda antenna array is presented.

II. DESIGN

Figure 1. shows the configuration for a two-element Yagi-Uda antenna array. The FET is used to provide a reactive output as a one-port circuit. The varying reactance provided through the change in the Schottky barrier as the gate bias is changed can be parallelly inserted to the slot antenna through electromagnetic coupling. With this additional reactance, an electronically tunable slot can be obtained. The input impedance of the reactive FET circuit is designed to be (0-j20) Ω around 10 GHz, which corresponds to 0.8 pF at 10 GHz. This input impedance is to be placed at the ends of the slot, where the impedance is low, so that it does not significantly affect the field distribution in the slot antenna. The impedance at the very end of the slot, however, is 0 Ω. Therefore, an offset of 0.067λ between the very end of the slot and the center of the microstrip line is implemented.

In order to provide a RF short at the crossing point of the slot and microstrip line, a capacitor is seriesly connected to the end of the microstrip line before it is grounded. Two $1\lambda_{sw}$ long slots are presented here. The spacing between two slot lines is $0.25\ \lambda_0$.

A two-element Yagi-Uda antenna array is built, as shown in Figures 2 and 3. As the DC biases imposed upon the gate and drain of the FET are changed, the slot #2 is increased in its resonant frequency while decreased in its electrical length, so that it can serve as a director. Thus, a two-element Yagi-Uda antenna array is achieved.

III. RESULTS

The slot, the reactive FET circuit and the feed line of the external source are fabricated on RT/duroid 5870 by ROGERS with ε_r=2.33 and 31 mils in thickness, and GaAs MESFET transistors manufactured by NEC (NE76184A) are used as the active devices in the circuit. The capacitors used are 2.4 pF.

The measured result of S11 of the reactive FET circuit is shown in Figure 4. The tuning voltages are 0V to –1.54V for the gate voltage (V_{gs}) and 0V to 0.36V for the drain voltage (V_{ds}). The variation of the resonant frequency mainly depends on the change of V_{gs}. Since the reactive FET has the reactive element on the source terminal, the operation is not quite stable as V_{ds} increases. Under small V_{ds}, however, it is possible to obtain wide tuning range.

A tuning range of 8% in resonant frequency of the reactive FET circuit is obtained. With this, we are able to change the electrical length of the slot by approximately the same amount. The resulting H-plane radiation pattern of the two-element Yagi-Uda antenna array is shown in Figure 5. With a DC bias of V_{gs}=-1.535 V and V_{ds}=0.35 V, a front-to-back ratio of 10 dB is observed. Without DC bias, only a slight directivity is observed, and the measured front-to-back ratio is 3 dB.

IV. CONCLUSION

In this work, a two-element Yagi-Uda antenna array with two physically equal-length elements is designed. Reactive FET circuits are utilized to tune the electrical length of one of the two slots. A tunable two-element Yagi-Uda antenna array is demonstrated, and a 10 dB front-to-back ratio is obtained. This work provides a novel idea that the mainbeam of Yagi-Uda antenna arrays can be made switchable by the utilization of reactive FET circuits.

ACKNOWLEDGEMENTS

The authors wish to thank Dr. S. Kawasaki and Dr. Chien-Nan Kuo for their precious technical advice. This project is supported by UCLA JSEP under contract F49620-92-C-0055.

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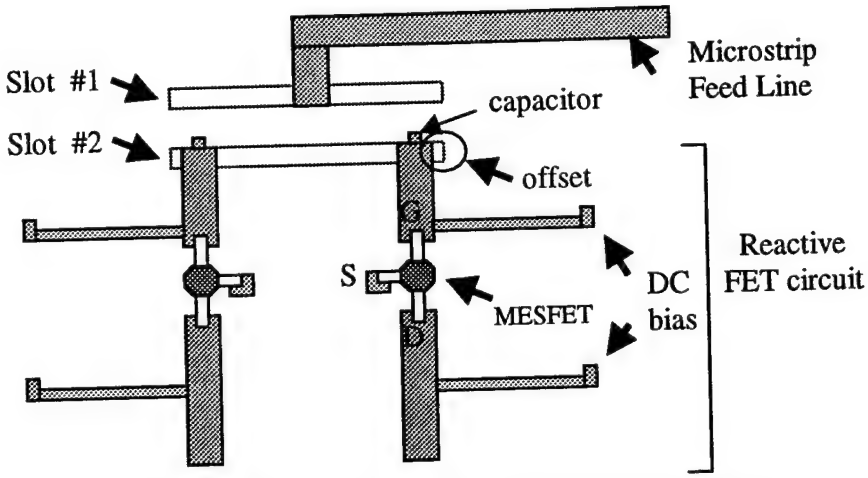

Figure 1. Configuration of a two-element Yagi-Uda slot array integrated with reactive FETs.

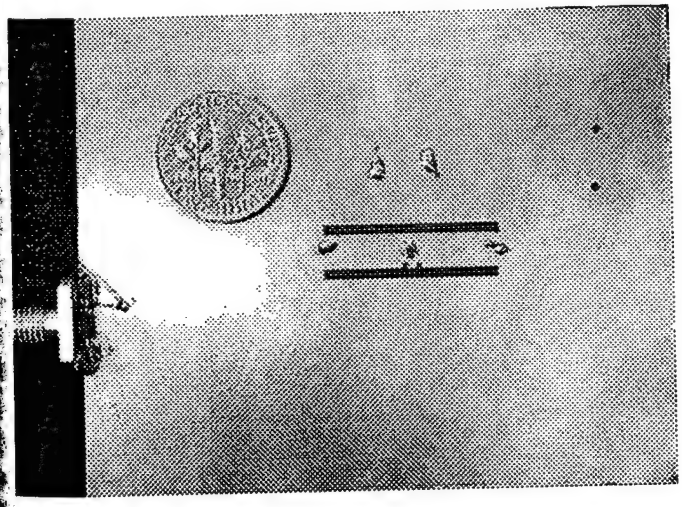

Figure 2. Slot lines side of the circuit.

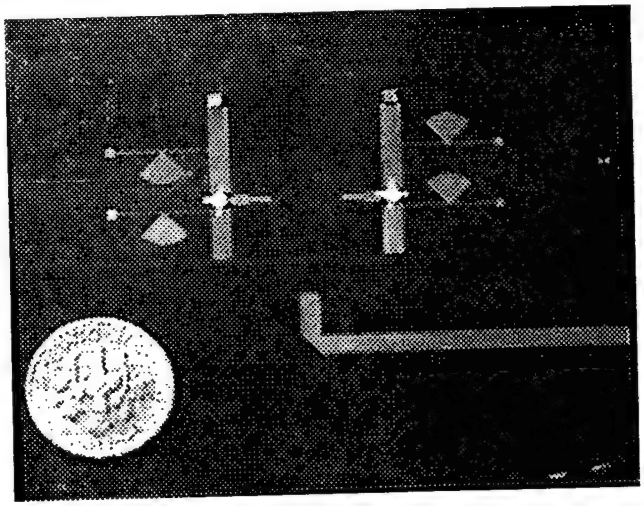

Figure 3. Microstrip line side of the circuit.

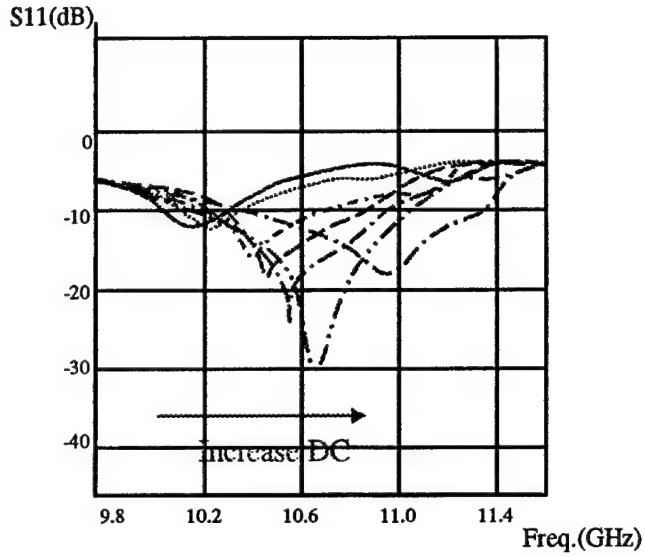

Figure 4. Shifting of S11 of the reactive FET circuit when DC bias is imposed.

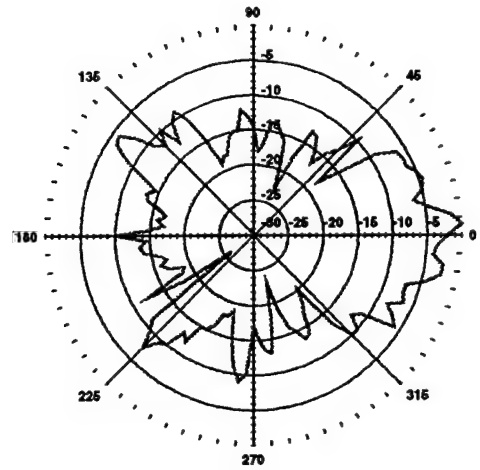

Figure 5. Radiation Pattern in H-plane with DC bias: Vgs=-1.535 V, Vds=0.35 V.

Table I. Comparison of front-to-back ratio with and without bias.

Without bias	3 dB
With bias	10 dB

sistently produce lower compression currents than time-domain measurements for all tested photodetectors. The difference can be explained by the delayed evolution of the space-charge field and by the fact that saturation is frequency dependent. High-frequency signals become saturated at much lower levels than low-frequency signals. Frequency-domain measurements are usually performed at high frequencies, whereas time-domain measurements represent the average saturation level over a broad frequency range. We report details of measurements, including the bias dependence, simulation results, buildup time of the space-charge field, and comparison between the time- and frequency-domain measurements.

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CThM3 **11:00 am**

Long-wavelength velocity-matched distributed photodetectors

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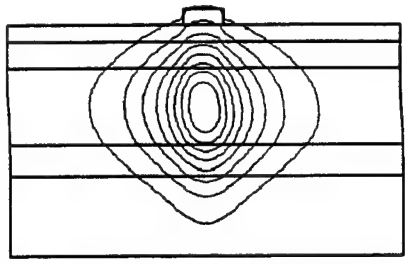
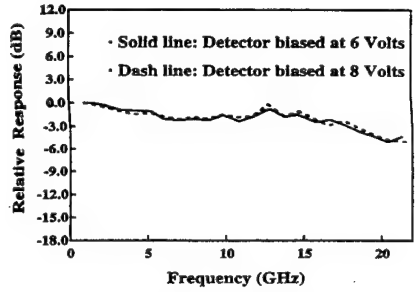
High-power, high-speed photodetectors are a key component in microwave fiber-optic links, optoelectronic generation of microwaves, and millimeter waves.[1] Previously, we have reported a GaAs/AlGaAs velocity-matched distributed photodetector (VMDP) that operates at 860 nm and demonstrated its potential for high-saturation photocurrents.[2] For applications in rf photonic systems, however, InP-based long-wavelength photodetectors operating at 1.3 or 1.55 μm are required. In this paper, we report on the experimental results of InGaAs/InAlGaAs/InP VMDP.



CThM3 Fig. 2. Contour plot of the fundamental mode field amplitude in the passive optical waveguide using BPM simulation. See Fig. 1 for layer structure.



CThM3 Fig. 3. Measured frequency response of long-wavelength VMDP (12 photodiodes, 1.2 mm long).

The schematic structure of the VMDP is illustrated in Fig. 1. Active metal-semiconductor-metal (MSM) photodiodes are periodically distributed on top of a passive optical waveguide. Optical signal is evanescently coupled from the passive waveguide to the active MSM photodiodes. Photocurrents generated from each MSM photodiode are added in phase through a 50-Ω coplanar strip (CPS) microwave transmission line that is velocity matched to the optical waveguide. The MSM photodiodes serve two functions here: they generate photocurrents and provide the periodic capacitance loading needed for velocity matching. The VMDP design allows the passive waveguide, the active photodiodes, and the microwave coplanar strips to be independently optimized. In Fig. 1, the active MSM photodiode consists of an InGaAs absorption layer, an InGaAs/InAlAs graded superlattice layers, and an InAlAs Schottky-barrier enhancement layer. At 10-V bias, a dark current of 190 pA is measured for an 11 × 48-μm^2 MSM photodiode. For a 1.2-mm-long VMDP with 12 11 × 48-μm^2 MSM photodiodes, a dark current of 25 nA is measured at 10-V bias.

Figure 2 shows the contour plot of the fundamental mode field amplitude in the passive waveguide using beam propagation method (BPM) simulation. The VMDP is designed so that only the fundamental mode exists in the optical waveguide and the active photodiode regions. Simulation results with the BPM method indicate a 4% scattering loss and 7% absorption loss per photodiode. Scattering loss can be reduced to 1% per diode by optimizing the geometric structure of the active photodiode. The device under test is 1.2 mm long and consists of 12 MSM photodiodes. In this experiment, optical lithography is employed to pattern the MSM photodiodes. Both the fingers and the spacing are 1 μm wide. After antireflection (AR) coating, a quantum efficiency of 34% was measured (this includes the coupling loss from optical fiber). High-saturation current measurement with a high-power erbium-doped fiber amplifier is in progress.

The frequency response of the VMDP is characterized by the optical heterodyne method.[4,5] The system consists of two external cavity tunable lasers at 1.55 μm; the frequency of each laser can be tuned in 1-GHz steps. The optical signals are combined by a 3-dB coupler and coupled to the VMDP through a fiber pickup head. The microwave signal generated by optical mixing in the VMDP is collected at the output end of the CPS by a 50-GHz picoprobe (GGB Industries), which is connected to an rf-power sensor and monitored by an rf-power meter. The calibrated frequency response of long-wavelength VMDP is shown in Fig. 3. A 3-dB bandwidth frequency of 18 GHz is measured. By scaling down the MSM to 0.1 μm scale, a frequency response >100 GHz is expected.

In summary, we have experimentally demonstrated a high-speed, high-power long-wavelength VMDP using optical lithography. A 3-dB bandwidth of 18-GHz and an overall quantum efficiency of 34% have been achieved.

This project is supported by TRW, ONR MURI on RF Photonics, ARO, JSEP, and UC MICRO.

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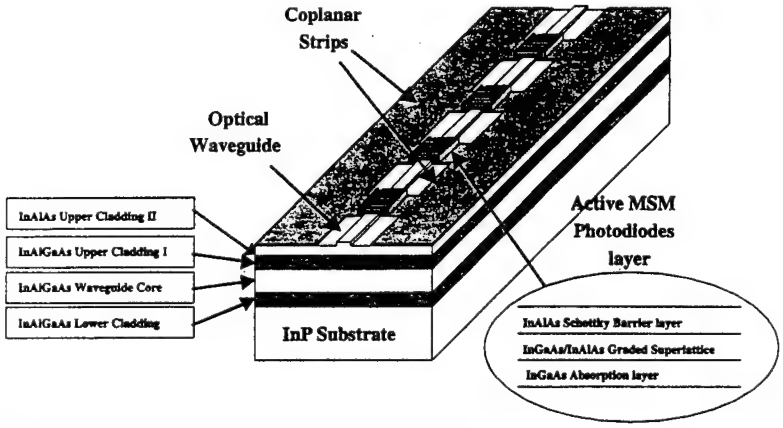

CThM3 Fig. 1. Schematic structure of long-wavelength velocity-matched distributed photodetector (VMDP).

the Fourier transform of the EO-signal is shown in Fig. 3. To correct the frequency response for the effect of finite duration of the optical sampling and excitation pulse, the Fourier transforms of their measured autocorrelation traces are used. A further effect on the system response results from the finite transit time of the sampling pulse in the electro-optically active InP substrate. Its response characteristic is calculated by accounting for the spatial distribution of the electric field of the CPW line, assuming quasi-TEM behaviour of the propagating signal. The resulting frequency response of the EO-sampling system as well as the corrected response of the detector are shown in Fig. 3. A 3dB bandwidth of 70GHz results from the corrected response characteristic. The comparison of the corrected response with the RC-limited response (also shown in Fig. 3), which is obtained from the capacitance (29fF) and series resistance (5Ω) of the detector when connected to a 50Ω transmission line, shows that, in the frequency range 120 and 170GHz, the response is dominated by the RC-effect. Moreover, the comparison indicates that the transit-time limited bandwidth of the devices exceeds 150GHz. The corrected response slightly exceeds the RC-limit at very high frequencies in Fig. 3. This may be attributed to the uncertainty of the correction procedure, which is estimated to be ±0.5dB.

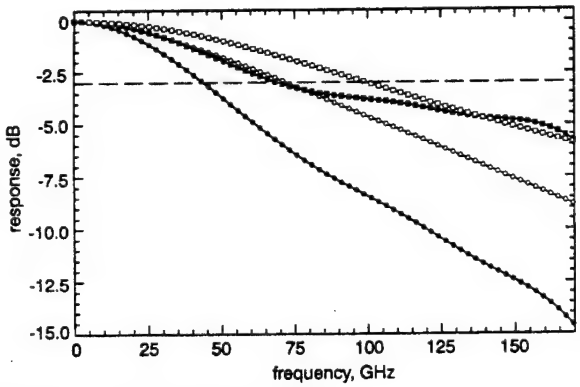

Fig. 3 *Frequency response characteristics*

■ corrected response
● uncorrected response
○ response of measuring system
□ RC limited response

Typically, the dark currents of the devices range between 1 and 2nA at 2V bias. The CW quantum efficiency of uncoated devices at 1.55 and 1.3μm is found to be 3.5 and 10%, respectively. The application of a silicon nitride AR coating leads to an enhanced efficiency of 6.7 and 17%, respectively. Note that the behaviour of the efficiency does not obey the geometric-optics approximation. Rather, its treatment requires the application of exact diffraction theory [4]. The polarisation dependence of the quantum efficiency is found to be < 0.2dB. Moreover, the AR coating gives rise to a larger capacitance of 40fF due to the increase in the effective dielectric constant. Thus, preserving the bandwidth of 70GHz with AR coated devices will require a reduction of the active area by ~30%. As recently demonstrated in conjunction with InGaAs MSM detectors [6], a drastic improvement of the quantum efficiency without a significant loss to bandwidth performance can be achieved by rear illumination in combination with resonant cavity enhanced (RCE) absorption. Such an RCE configuration is expected to result in a quantum efficiency of ~40% at 1.55μm.

Conclusion: Front-side illuminated 14μm active area diameter InGaAs photodetectors for high-speed and polarisation-insensitive operation have been fabricated. The devices possess 0.2μm feature size finger electrodes with a semicircular shape. A pulse response time of 3.8ps at 2V bias has been measured by EO-sampling at 1.55μm wavelength. The corrected frequency response exhibits a 3dB bandwidth of 70GHz.

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Long wavelength velocity-matched distributed photodetectors for RF fibre optic links

T. Chau, L. Fan, D.T.K. Tong, S. Mathai, M.C. Wu, D.L. Sivco and A.Y. Cho

An InP-based long wavelength velocity-matched distributed photodetector with metal-semiconductor-metal photodiodes is experimentally demonstrated. A 3dB bandwidth of 18GHz and an external quantum efficiency of 0.42A/W have been achieved.

Introduction: High power, high frequency photodetectors are a key component for high performance microwave fibre optic links [1 – 3]. High optical power in externally modulated links can greatly enhance the link gain, signal-to-noise ratio, and the spurious-free dynamic range [4]. It is also very useful for millimeter-wave generation by photomixing. Previously, we have reported a GaAs/AlGaAs velocity-matched distributed photodetector (VMDP) operating at 860nm wavelength, and demonstrated its potential for high saturation photocurrent [1]. For applications in RF photonic systems, however, InP-based long-wavelength photodetectors operating at 1.3 or 1.55μm are required. The successful fabrication of a long-wavelength VMDP is first reported in [5]. In this Letter, we report on the experimental results and RF performance of the InGaAs/InAlGaAs/InP VMDP.

Device structure and fabrication: The schematic structure of the VMDP is illustrated in Fig. 1*a*. Active metal-semiconductor-metal (MSM) photodiodes are periodically distributed on top of a passive optical waveguide. The optical signal is evanescently coupled from the passive waveguide to the active MSM photodiodes. Photocurrents generated from the MSM photodiodes are added in phase through a 50Ω coplanar strip (CPS) microwave transmission line that is velocity-matched to the optical waveguide. The MSM photodiodes serve two functions: generating photocurrents and providing the periodic capacitance loading needed for velocity matching. The VMDP design allows the passive waveguide, the

active photodiodes, and the microwave coplanar strips to be independently optimised. The active MSM photodiodes consist of an InGaAs absorption layer, InGaAs/InAlAs graded superlattice layers, an InAlAs Schottky-barrier enhancement layer, and a Ti/Au contact with 200Å/2000Å thickness. The fabrication process is as follows: first, Ti/Au interdigitated fingers with 1.5μm width and 0.5μm spacing are patterned using standard photolithography and liftoff techniques, then active mesas for individual photodiodes are defined by wet etching down to the InAlAs upper cladding II. Fig. 1*b* shows the cross-section of the VMDP after mesa etching. A passive ridge waveguide with a ridge height of 0.1μm is employed to connect the photodiodes. After mesa and waveguide etching, the CPS microwave transmission line is patterned using a standard liftoff technique.

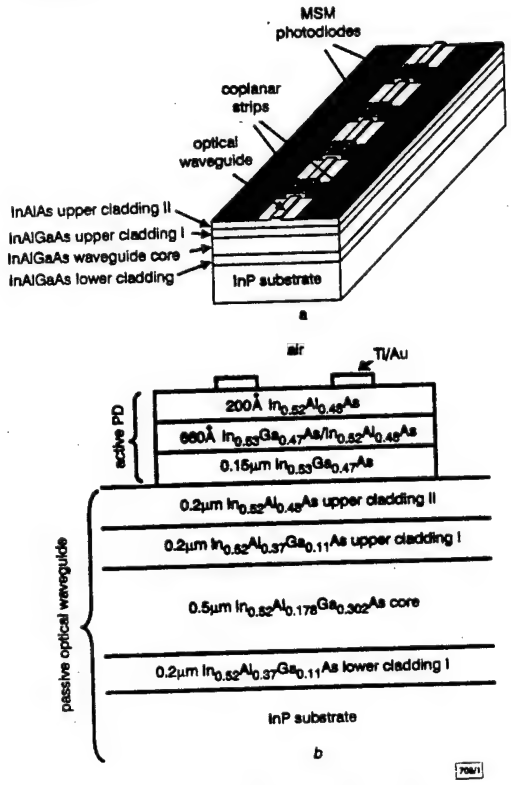

Fig. 1 *Schematic structure of long-wavelength VMDP and cross-section after mesa etching*

a Schematic structure of VMDP
b Schematic cross-section of VMDP after mesa etching

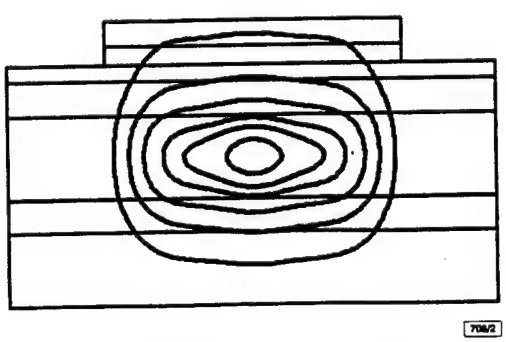

Fig. 2 *Contour plot of fundamental mode field amplitude in photodiode region using BPM simulation*

See Fig. 1 for detailed layer structure

The beam propagation method (BPM) is used to design and simulate the optical performance of the VMDP. A large-core optical waveguide is employed to reduce the coupling loss between the passive waveguide and the photodiode region as well as to reduce the optical power density in the absorption region. Only the fundamental mode exists in both the passive waveguide and the photodiode regions. Fig. 2 shows the optical field distribution of the VMDP in the photodiode region. Most of the optical energy is concentrated in the waveguide core. The optical absorption and the coupling loss per photodiode for the VMDP with 11μm long photodiodes and 89μm spacing between photodiodes are estimated to be 6.2% and 1.8%, respectively, by the BPM simulation. The coupling loss can be further improved by reducing the width of the active mesa.

Device characteristics: The finished devices are cleaved and mounted on copper heat sinks before testing. The VMDP exhibits a very low dark current: 190pA at 10V bias for individual photodiodes (11 × 48μm²), and 25nA for the 1.2mm long VMDP with 12 photodiodes. The excess dark current in the VMDP is attributed to the leakage current under the CPS electrodes, which has a much larger area than the active photodiodes. This can be eliminated by placing the electrodes on thin dielectric. The external quantum efficiency is measured to be 0.42A/W after anti-reflection (AR) coating. The dominant loss comes from the coupling from the optical fibre to the VMDP. All devices exhibit linear responsivity up to 12mA of photocurrent.

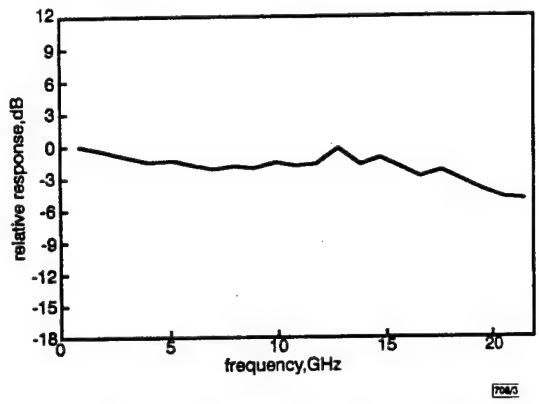

Fig. 3 *Measured frequency response of long wavelength VMDP*

12 photodiodes, total length = 1.2mm

The microwave performance of the VMDP is measured by an HP 8510C network analyser. The microwave return loss (S_{11}) is <−22dB from 0.1 to 40GHz. The characteristic impedance of the VMDP is matched very well to 50Ω (within 4%) for the entire frequency range. The frequency response of the VMDP is characterised by the optical heterodyne method [6, 7] using two external cavity tunable lasers at 1.55μm. The optical signals are combined by a 3dB coupler, and coupled to the VMDP through a fibre pickup head. The output microwave is collected by a 50GHz picoprobe (GGB Industries) and monitored by an RF power meter. The calibrated frequency response of the VMDP is shown in Fig. 3. A 3dB bandwidth of 18GHz is measured. The bandwidth is limited by the transit time of the MSM photodiodes. By scaling down the MSM to a 0.1μm scale, much higher bandwidth (> 100GHz) can be obtained.

The maximum photocurrent of 12mA is currently limited by thermal damage to the MSM photodiode. The device remains linear up to the maximum photocurrent. Inspection of the failed device by energy dispersive X-ray analysis (EDX) indicates that gold difflision into the semiconductor is the main failure mechanism. Improving the diffusion barrier of the Schottky contact should lead to even higher photocurrent.

Conclusion: We have experimentally demonstrated a long wavelength velocity-matched distributed photodetector with twelve metal-semiconductor-metal photodiodes. A 3dB bandwidth of 18GHz and an external quantum efficiency of 0.42A/W have been achieved.

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Optoelectronic clock recovery circuit using resonant tunnelling diode and uni-travelling-carrier photodiode

K. Murata, K. Sano, T. Akeyoshi, N. Shimizu, E. Sano, M. Yamamoto and T. Ishibashi

An optoelectronic clock recovery circuit is reported that monolithically integrates a resonant tunnelling diode and a uni-travelling-carrier photodiode. The integrated circuit extracts an electrical 11.55GHz clock signal from 11.55Gbit/s RZ optical data streams in a wide locking range with low power dissipation. Furthermore, the extraction of a subharmonic clock from 23.1 and 46.2Gbit/s input data streams is also confirmed.

Introduction: Because of the growth in multimedia services, ultra-high-speed optical receivers will be indispensable for future backbone networks. To realise a small high-speed receiver circuit with low power consumption, an optoelectronic circuit using resonant tunnelling diodes (RTDs), and a new type of wideband, high-saturation power photodetector called the uni-travelling-carrier photodiode (UTC-PD) [1] is a promising candidate because of its inherent high-speed operation. For example, an RTD/UTC-PD integrated circuit (IC) demultiplexing an 80Gbit/s optical signal into 40 Gbit/s electrical signals at an extremely low power of 7.75mW has been demonstrated [2]. A clock recovery circuit is another key component for realising the receiver circuit. Several kinds of optical injection-locked RTD oscillator [3 – 5] have been reported, and phase locking to optical input has been demonstrated. However, clock extraction from an optical data signal, such as a pseudo-random bit stream (PRBS), and subharmonic clock extraction have not been reported.

This Letter describes an optoelectronic clock recovery circuit that monolithically integrates an RTD and a UTC-PD on an InP substrate. The principle of synchronisation is optical injection-locking of a free-running oscillator. The fabricated circuit successfully extracted an electrical 11.55GHz clock signal from an 11.55Gbit/s RZ optical input data stream in a wide locking range with low power dissipation. Furthermore, the IC exhibited subharmonic clock extraction from 23.1Gbit/s and 46.2Gbit/s input data streams.

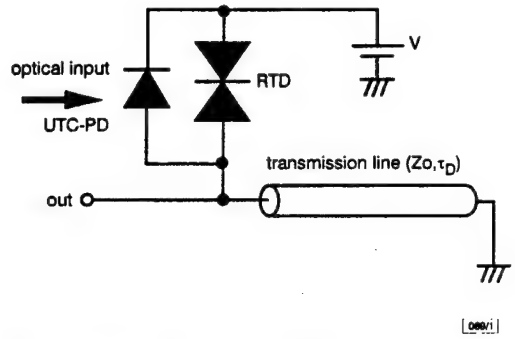

Fig. 1 *Circuit diagram of clock recovery circuit*

Circuit configuration: Fig. 1 shows a circuit diagram of the proposed clock recovery circuit. The circuit consists of an oscillator, which is constructed with an RTD and a transmission line, and a UTC-PD. In the RTD oscillator, the RTD is biased in the negative differential resistance (NDR) region, and the collector is connected to the transmission line whose other terminal is connected to the ground. The essential synchronisation principle is injection-locking of the RTD oscillator using the photocurrent generated by the UTC-PD. Here, the use of the UTC-PD is important to maintain fast photoresponse at low bias voltages [6] corresponding to the NDR region of the RTD. The self-oscillation of the RTD oscillator is theoretically analysed in [7], and the oscillating frequency is inversely proportional to the propagation delay time τ_D of the transmission line. In the present circuit, the transmission line is a coplanar wave guide monolithically fabricated on the InP substrate. The physical length and characteristic impedance Z_0 of the transmission line were 1150μm and 50Ω, respectively. The active areas of the RTD and UTC-PD were 6 and 20μm², respectively. The bias voltage V was +0.43V; the chip size was 1.9 × 0.5mm.

Experimental results: The IC was fabricated by monolithically integrating an InGaAs/AlAs/InAs RTD and an InP/InGaAs UTC-PD on an semi-insulating InP substrate [2, 8]. The peak and valley current of the RTD were 7.4mA at 0.35V and 0.6mA at 0.7V, respectively. The responsivity of the UTC-PD was 0.26A/W at a wavelength of 1.55μm, and the 3dB bandwidth around the bias voltage V was ~ 80GHz.

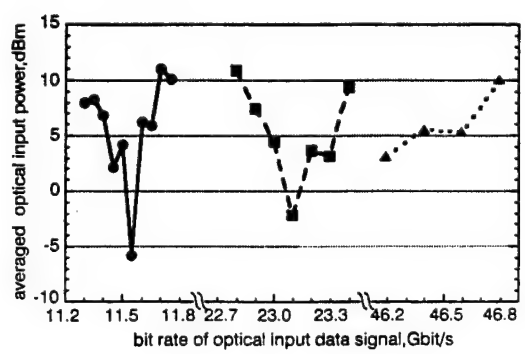

Fig. 3 *Locking range of clock recovery circuit*

● fundamental
■ first-order harmonic
▲ third-order harmonic

The IC was tested on a wafer. The input RZ optical data stream (λ = 1.55μm) was generated by an electro-optic pulse pattern generator that can output a 10–80Gbit/s optical data stream [9]. The pulsewidth of the RZ optical data input was < 10ps, and the data sequence was PN 2^{23}–1 PRBS. The input optical signal illuminated

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High Performance Long-Wavelength Velocity-Matched Distributed Photodetectors For RF Fiber Optic Links

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Abstract

Improved performance of InP-based long wavelength velocity-matched distributed photodetector (VMDP) with metal-semiconductor-metal photodiodes is experimentally demonstrated. A 3-dB bandwidth of 13 GHz and an external quantum efficiency of 0.57 A/W have been achieved.

I. Introduction

High power, high frequency photodetector is a key component for high performance microwave fiber optic links [1-3]. High optical power in externally modulated links can greatly enhance the link gain, signal-to-noise ratio, and spurious-free dynamic range [4]. In conventional photodetectors, there is a trade-off between the saturation photocurrent and the device bandwidth. High power device requires a large absorption volume, thus the device is usually large, resulting in large RC time or long carrier transit time that limits the device bandwidth. In contrast, conventional high-speed photodetectors with small RC time and small transit time usually have low saturation photocurrents. The velocity-matched distributed photodetectors (VMDP) is a novel type of travelling wave photodetector which can achieve both high bandwidth and high saturation power. It was first proposed in 1993 [6], and has been successfully demonstrated experimentally [1,5]. The successful fabrication of long-wavelength VMDP for use in 1.3 or 1.55 μm RF Photonics systems was first reported in [5]. In this paper, we report on the performance of improved long wavelength VMDP with new design and fabrication procedures. A 3-dB bandwidth of 13 GHz and an external quantum efficiency of 0.57 A/W have been achieved.

II. Device Structure and Fabrication

The schematic structure of the VMDP is illustrated in Figure 1. A passive (non-absorbing) optical waveguide is used to serially connect an array of periodically spaced metal-semiconductor-metal (MSM) photodiodes. Light in the optical waveguide is evanescently coupled to the MSM photodiodes. The photocurrents are added in phase and collected by a 50Ω coplanar strips (CPS) microwave transmission line. The active photodiodes are designed to have small optical confinement factor to keep them bellow saturation under high optical illumination. The bandwidth of the VMDP is limited by that of the individual photodiode, and the residual velocity mismatch. Since photocurrents are collected from many photodiodes along the transmission line, the individual photodiode does not need to have high quantum efficiency and therefore can be made small and fast. The MSM photodiodes serve two functions: generating photocurrents as well as providing the periodic capacitance loading needed for velocity matching. The VMDP design allows the passive waveguide, the active photodiodes, and the microwave coplanar strips to be independently optimized.

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The principle of the VMDP has been discussed in more detail in [1]. We have made three major changes: (1) mesa width reduction to reduce optical coupling loss from optical waveguide to active MSM photodiodes; (2) nitride passivation on mesa sidewall and underneath the large CPS electrodes to reduce dark current and improve device reliability; and (3) use of platinum in Schottky metal contacts to prevent gold diffusion at high power operation

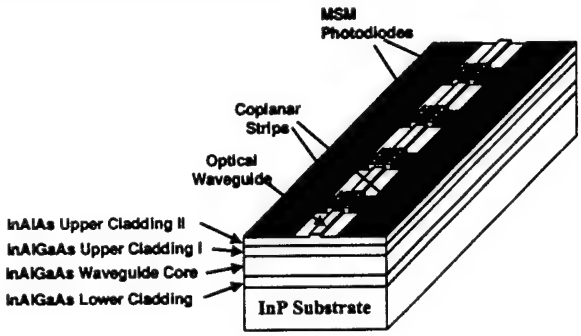

Figure 1. Schematic structure of long-wavelength velocity-matched distributed photodetector (VMDP)

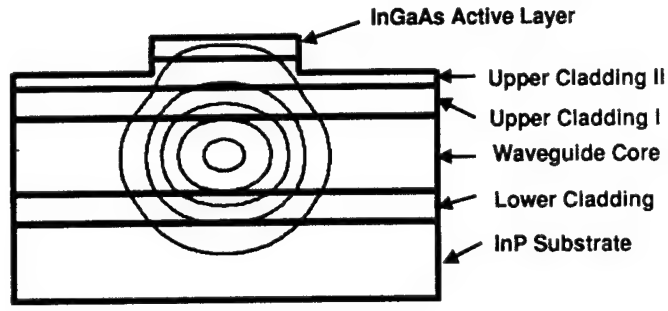

Figure 2. Contour plot of the fundamental mode profile in the photodiode region using BPM

Beam propagation method (BPM) is used to design and simulate the optical performance of the VMDP. Large-core optical waveguide is employed to reduce the coupling loss between the passive waveguide and the photodiode region as well as to reduce the optical power density in the absorption region. Only fundamental mode exists in both the passive waveguide and the photodiode regions. Figure 2 shows the optical field distribution of VMDP in the photodiode. Most of the optical energy concentrates in the waveguide core. The optical absorption and the coupling loss per photodiode for the VMDP shown in Fig. 1 are estimated to be 8.3% and 1.6%, respectively, by the BPM simulation.

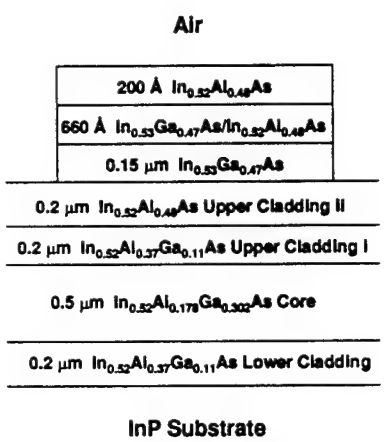

Figure 3. Cross section of VMDP wafer after mesa etching

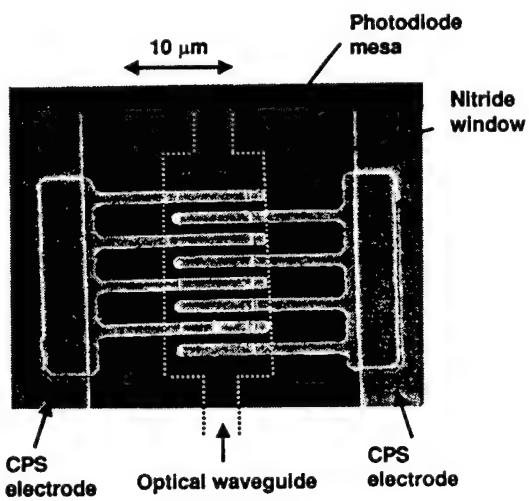

Figure 4. SEM picture of a single MSM photodiode of VMDP

The active MSM photodiodes consists of InGaAs absorption layer; InGaAs/InAlAs graded superlattice layers; InAlAs Schottky-barrier enhancement layer; and interdigitated fingers. The fabrication process is as followed: first, metal alignment markers are patterned on the substrate for subsequent process. Next, active mesas for photodiodes are defined by wet etching down to the InAlAs Upper Cladding II. Then optical ridge waveguide with ridge height

of 0.1μm is formed by wet etching. After mesa and waveguide etching, a Si_3N_4 passivation layer is deposited to protect the mesa edges. The nitride directly on top of the active mesas are opened for Schottky contacts. Interdigitated Ti/Pt/Au fingers with 1μm finger width and 1μm finger spacing are patterned in the open windows using optical lithography. Finally, the CPS microwave transmission line is fabricated using standard liftoff technique. The cross section of VMDP wafer after mesa etching is shown in Figure 3. Figure 4 shows the scanning electron micrograph (SEM) of a single MSM photodiode in the VMDP.

III. Device Characteristics

All devices under test are mounted on copper heat sinks. The temperature is set at 19 °C using a temperature controller. The VMDP exhibits very low dark current: 8.3 nA at 10V bias for a 1-mm-long VMDP with 13 photodiodes. The dark current has been reduced by 10 times compared to the VMDP in [5]. It is attributed to the nitride passivation which prevents the leakage currents through the sidewalls and the CPS electrodes. The external quantum efficiency is measured to be 0.4 A/W. With anti-reflection (AR) coating, it could reach 0.57 A/W. The dominant loss comes from the coupling from optical fiber to the VMDP. Figure 5 shows the DC responsivity of the new device. The responsivity of the VMDP in [5] is also shown for comparison.

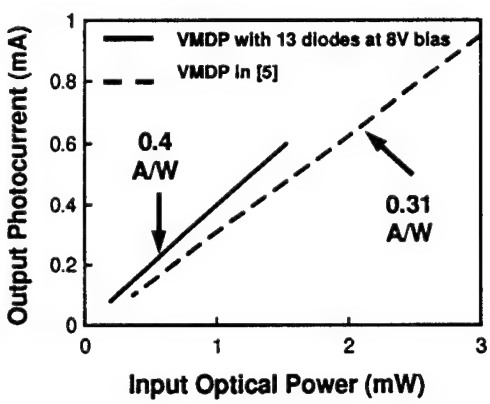

Figure 5. DC responsivity of VMDP (without AR coating)

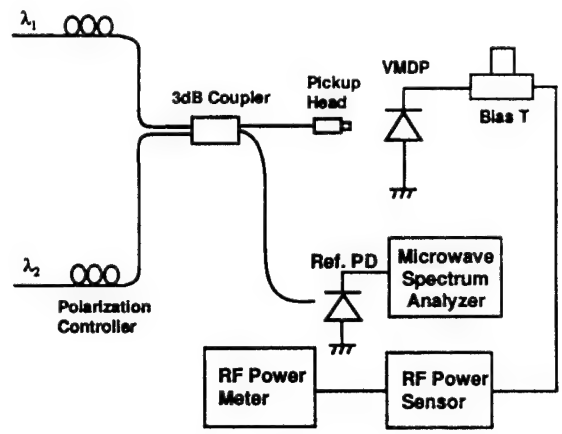

Figure 6. Schematic of optical heterodyne system setup for frequency response characterization of VMDP

The frequency response of the VMDP is characterized by optical heterodyne method [7,8]. The schematic of the experimental setup is shown in Figure 6. The system consists of two external cavity tunable lasers at 1.55μm, the frequency of each laser can be tuned in 1GHz step. The optical signals are combined by a 3dB coupler, and coupled to the VMDP using a fiber pickup head. The microwave signal generated by optical mixing in the VMDP is collected at the output end of the CPS by a 50GHz picoprobe (GGB Industries), which is connected to an RF power sensor and monitored by an RF power meter. The calibrated frequency response of long wavelength VMDP is shown in Figure 7. At 10 Volt bias, a 3dB bandwidth frequency of 13GHz is measured. By scaling down the MSM to deep sub-micron scale, much higher bandwidth (> 100 GHz) is expected.

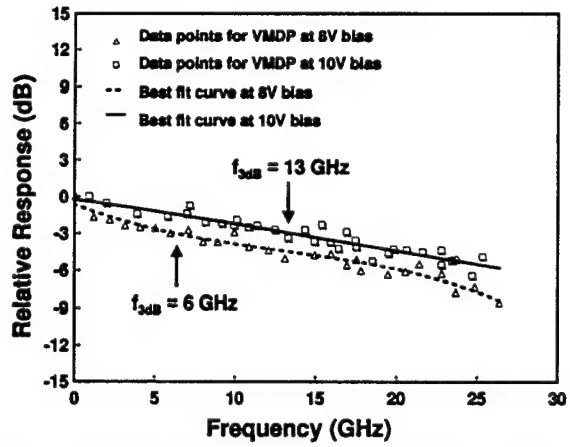

Figure 7. Measured frequency response of a long wavelength VMDP with 10 MSM photodiodes at different DC bias voltages

IV. Conclusion

In summary, we have experimentally demonstrated the improved performance of the long wavelength velocity-matched distributed photodetector (VMDP). A 3dB bandwidth of 13 GHz and a responsivity of 0.57 A/W have been achieved.

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Distributed Balanced Photodetectors for High Performance RF Photonic Links

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Abstract

A novel velocity-matched distributed *balanced* photodetector with a 50Ω coplanar waveguide output transmission line has been experimentally demonstrated in the InP/InGaAs material system. Distributed absorption and velocity matching are employed to achieve high saturation photocurrent. A common mode rejection ratio greater than 27 dB has been achieved. The RF link experiment conducted at 6.48 GHz shows that the laser intensity noise has been suppressed by more than 17 dB.

Index Terms

RF photonics, microwave photonics, noise suppression, analog fiber optic links, balanced photodetectors, optical receivers

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I. INTRODUCTION

Balanced photodetectors are of great interest to analog fiber optic links because they can suppress laser relative intensity noise (RIN) and amplified spontaneous emission noise (ASE) from erbium-doped fiber amplifiers (EDFA) [1]. Because balanced photodetectors can achieve shot noise-limited link performance, we can continue to improve the noise figure and the spurious-free dynamic range (SFDR) of externally modulated links by increasing the power of the optical carrier. Therefore, balanced photodetectors with broad bandwidth and high saturation photocurrents are particularly important for analog fiber optic link applications. Though discrete balanced photodetectors with high saturation power have been reported, their bandwidth is limited [2]. Most of the reported integrated balanced receivers suffer from low saturation power and are not suitable for analog links [3-5]. Previously, we have reported a velocity-matched distributed photodetector (VMDP) with a peak saturation photocurrent of 56 mA and a 3-dB bandwidth of 49 GHz [6]. Recently, InP-based long wavelength VMDP has also been reported [7]. Compared with other photodetector structures, the VMDP is more suitable for implementing balanced photodetection since it has separate optical and microwave waveguides. In this paper, we propose and demonstrate a novel, monolithic distributed balanced photodetector that can simultaneously achieve high saturation photocurrent and large bandwidth. A common mode rejection ratio of 27 dB and a noise suppression of 17 dB have been experimentally demonstrated.

II. DESIGN

Figure 1 shows the principle and the schematic structure of the distributed balanced photodetector. It consists of two input optical waveguides, two arrays of high-speed metal-semiconductor-metal (MSM) photodiodes distributed along the optical waveguides, and a 50Ω coplanar waveguide (CPW) output transmission line. The detector operates in balanced mode when a voltage bias is applied between the two ground electrodes of the CPW. The common-mode photocurrent flows directly to the bottom ground electrode while the difference photocurrent (signal) flows to the center conductor. The signal is then collected by the CPW. The diodes are 23 μm long and 5 μm wide. The separation between photodiodes is 150 μm. The MSM fingers with 1μm width and 1μm spacing are patterned by optical lithography. The overlap of the MSM fingers is 10.5 μm. The central conductor of the CPW has a width of 55 μm and the separation between the central conductor and the ground conductors is 85 μm. Without the photodiodes, the velocity of the CPW is about 31.8% faster than the light velocity in the optical waveguide. The photodiode arrays provide the periodic capacitance loading to slow down the microwave velocity. By adjusting the length and separation of photodiodes, velocity matching between the CPW and the optical waveguides is achieved. The impedance of CPW is also matched to 50Ω.

The distributed balanced photodetector inherits the basic advantages of the VMDP, namely, high saturation photocurrent, high quantum efficiency, and large bandwidth. It should be noted that even though only the difference current (AC signal) is collected in the balanced photodetector, the DC light is still absorbed in the photodiodes. As a result, high DC saturation photocurrent is required for the distributed balanced photodetectors. By coupling only a small fraction of light from the passive waveguide to each individual photodiodes, the photodiodes are kept below saturation even under intense optical input. Though longer absorption length is required, the bandwidth of the distributed balanced photodetector remains high because of the velocity matching. The linearity of the detector is also improved by distributed absorption because the photo carrier density is reduced in the active region.

Optical Waveguide

The optical waveguide consists of the following: a 200-nm-thick $In_{0.52}Al_{0.37}Ga_{0.11}As$ lower cladding layer, a

500-nm-thick $In_{0.52}Al_{0.178}Ga_{0.302}As$ core region, a 200-nm-thick $In_{0.52}Al_{0.37}Ga_{0.11}As$ first upper cladding layer, and a thin $In_{0.52}Al_{0.48}As$ second upper cladding layer. The 150-nm-thick absorption region is located on top of the waveguide for evanescent coupling. Since the Schottky barrier height of most metals on InGaAs is typically between 0.2-0.3 eV, an $In_{0.52}Al_{0.48}As$ cap layer is used to increase the Schottky barrier height and therefore decrease the dark current of the photodiodes [8,9]. A graded layer is incorporated in the structure to reduce the minority carrier trapping at the InAlAs-InGaAs band edge discontinuity.

A scalar three-dimensional beam propagation method (BPM) was used to simulate the optical properties of the balanced VMDP. The absorption per photodiode and the optical coupling loss between photodiodes are estimated to be 8.8% and 3.2%, respectively. Our simulation shows that an AC quantum efficiency of 42% can be achieved for balanced receiver with 10 pairs of photodiodes. Since the two optical waveguides are 140 μm apart, no optical coupling between the waveguides is expected. This is confirmed by the BPM simulation. Figure 2 shows the optical intensity profile and the power distribution along the waveguides when a fundamental mode is launched into the first waveguide (WG1) at the input. The waveguide powers were calculated using computational windows surrounding the individual waveguides. Indeed, no power coupling to WG2 is observed. The slight decay in WG1 (0.195 dB/mm) is attributed to loss to slab mode.

Modeling of Microwave Transmission Line

The impedance and the phase velocity of the CPW are calculated using the equivalent circuit model described in Ref. [10]. The length of the photodiodes and the separation between them are adjusted to achieve simultaneous velocity matching and impedance matching. Since the separation between the central conductor and the ground electrodes (85 μm) are much smaller than the wavelength of the RF signal (about two order of magnitude smaller at 50 GHz), quasi static analysis is reasonably accurate [11]. The capacitors and resistors of each photodiodes are considered as lumped elements in our quasi-static simulation. After optimizing the receiver structure, a full-wave analysis was performed to verify the design. We found that the quasi-static results agree very well with the full wave analysis for frequency below 100 GHz. The period in our device corresponds to a cut-off frequency of 300 GHz, well above our expected frequency of operation. Therefore, the dispersion due to the periodicity of the structure is negligible for frequencies below 100 GHz [12].

The overall performance of the balanced VMDP is simulated using the model in Ref. [13], which includes the transit-time frequency response of the photodiodes, the loss and dispersion of the microwave transmission line, the optical coupling loss between the photodiodes, and the residue velocity mismatch between the CPW and the optical waveguides.

III. FABRICATION

Fabrication of the receiver started with removing the InGaAs layer except in the active areas of the photodiodes. Ridge waveguides with 100 nm ridge height were formed by wet chemical etching. The active regions of the photodiodes were defined by opening 6×23-μm^2 windows on the 150-nm-thick silicon nitride (Si_3N_4) film deposited by plasma-enhanced chemical vapor deposition (PECVD). Buffer HF was used to open the windows. The Ti-Au electrodes and contact pads were then delineated by standard lift-off processes. The tips of the MSM fingers are placed on top of the Si_3N_4 to suppress the soft breakdown and enable the MSM diodes to operate over a wider range of bias voltages [14]. A 350-nm-thick coplanar waveguide was formed by standard lift-off process to connect the distributed balanced photodetectors. Finally the balanced detector structure is cleaved and mounted on copper heat sinks. By measuring the forward current-voltage characteristics, the barrier height of the metal-semiconductor junction was estimated to be 0.57 eV.

IV. EXPERIMENTAL RESULTS

The balanced VMDP exhibits very good electrical and optical characteristics. The dark current is measured to be 28 $\mu A/cm^2$ at 10 V bias; the lowest reported for InAlAs/InGaAs MSM photodiodes (Figure 3). At the operating voltage of 4 V, the total dark current of a balanced receiver with 5 pairs of photodiodes is 1.5 nA. We used a pair of lensed fibers to couple light into the photodetector. Figure 3 also shows the measured responsivity of the photodetector as a function of bias voltage. The average DC responsivity was measured to be 0.45 A/W at 8 V bias. Responsivity as high as 0.6 A/W has been observed in some devices. With anti-reflection coating, the average responsivity can be increased to 0.64 A/W. The DC photocurrent at 8 V versus the input optical power is shown in Figure 4. The photocurrent of each VMDP remains linear up to 12 mA (27 mW of optical power). We did not increase the optical power further to avoid damaging the devices.

An HP 8510C network analyzer was used to measure the characteristic impedance and the microwave return loss (S_{11}) of the balanced receiver. Figure 5 shows the measured S parameters of the receiver. The S_{11} is below -30 dB from 45 MHz to 40 GHz, indicating that the impedance of the detector is very well matched to 50 Ω. The loaded CPW has very low insertion loss. The measured S_{12} shows a drop of only 0.6 dB from 45 MHz to 40 GHz.

The frequency response of the balanced VMDP was first characterized with light coupled to one waveguide only. Figure 6 shows the frequency response of the photodetector. Using the optical heterodyne technique with two external cavity tunable semiconductor lasers at 1.55 μm, the 3-dB bandwidth was found to be 16 GHz for both photodetector arrays. The bandwidth is currently limited by the carrier transit time of the MSM photodiodes. Since the

bandwidth of our capacitance loaded CPW is much greater than 40 GHz, the bandwidth of the balanced VMDP can be increased by scaling down the MSM photodiodes. Theoretical simulation indicates that bandwidth > 100 GHz is achievable.

Figure 7 depicts the experimental setup for balanced detection. A distributed feedback (DFB) laser with 1542-nm wavelength and 0 dBm output power is employed as optical source. It is amplified by an EDFA and then filtered by an optical bandpass filter with 2-nm bandwidth. The microwave signal was modulated onto the optical carrier by an X-coupled Mach-Zehnder modulator (MZM), which produces two complimentary outputs for the balanced VMDP. The outputs are coupled to the balanced VMDP by two lensed fibers. To maximize the signal enhancement and noise cancellation, it is important to match the amplitudes and phases of the two detected microwave signals. In our experiment, a variable attenuator was used to match the amplitudes of the photocurrents. Typical balance between the VMDP was within 2% of the total photocurrent reading. We also employed a variable optical delay line to match the microwave phases of the detected signals. For balanced detection, the RF signals need to be exactly 180° out of phase. The maximum delay in our setup is 50 mm, which allows us to match the phases of RF signals above 6 GHz.

Balanced detection is achieved by applying a bias of 8 V between the two ground electrodes of the CPW. A custom-made high-frequency probe with an integrated DC-blocking capacitor on one ground probe is used to collect the microwave output signal. Figure 8 shows the biasing scheme. The DC photocurrents are measured through two ammeters: the difference photocurrent (i_{DIFF}) is monitored through the bias-T connected to the probe, and the common mode photocurrent (i_{COM}) is monitored between the ground electrodes of the CPW. Figure 9 shows the common mode rejection ratio (CMRR), defined as $CMRR = 20 \cdot \log\left(\frac{i_{COM}}{i_{DIFF}}\right)$, as a function of the total photocurrent. Very high CMRR (> 27 dB) is measured for a wide range of photocurrent from 30 nA to 12 mA. This is attributed to the well-matched characteristics of the photodiodes in our monolithic balanced detectors.

To verify the balanced detection, we modulated the optical input at 8 GHz and varied the delay of the fiber optic delay line from 0 to 50 mm. Figure 10 shows the detected RF signal versus the delay. When the received RF signals have a 0° phase difference, the RF output is cancelled out in balanced mode. When the detected RF signals are 180° out of phase, the small signal photocurrents from the two photodiode arrays are added in phase and maximum RF signal is observed. The extinction ratio is more than 44 dB.

One key advantage of the balanced photodetector is its ability to cancel out the laser RIN. To evaluate the cancellation ratio of our device, we compare the noise spectra of a DFB laser measured by our photodetector in the unbalanced and the balanced modes. The DFB laser operates in CW condition and has a RIN peak at 6.5 GHz. The top trace in Figure 11 shows the noise spectra measured near its RIN peak when only one waveguide is illuminated. We confirm that the noise is dominated by the RIN of the DFB laser. When the optical input power is doubled, the noise floor increases by 6 dB. We then biased the photodetector in the balanced mode and coupled the input to both the optical waveguides. The bottom trace in Fig. 10 shows the noise spectra detected by the balanced detector. Suppression of the RIN by as much as 15 dB is observed. The maximum suppression occurs at 6.48 GHz, at which frequency the phases of the detected noise matches exactly. Since optical path lengths of the two input fibers are not equal (due to the insertion of the fiber delay line), the cancellation of the laser RIN is not as effective when the frequency deviates from 6.48 GHz. With equal fiber lengths for both inputs, uniform noise cancellation is expected for all the frequencies.

Figure 12 shows the RF spectra of the output from the balanced VMDP in the unbalanced (only one waveguide is illuminated) and the balanced mode. Suppression of the noise floor by 17 dB has been observed in the balanced mode over a wide frequency range from 6 to 15 GHz. This is equivalent to 23 dB improvement of noise if two outputs were considered. The signal is also enhanced by 6 dB. For frequencies below 6 GHz, the fiber length for one RF period is longer than 50 mm, exceeding the maximum delay length in our current setup. We are currently working on a new setup with two fiber optic delay lines to achieve exactly equal optical path lengths for broad band operation without any tuning of the delay line. This will allow us to measure the AC responsivity of the device in the balanced mode.

V. CONCLUSION

We have successfully designed, fabricated, and experimentally demonstrated a balanced velocity-matched distributed photodetector (VMDP) with both impedance and velocity matching. The device exhibits a very low dark current (1.5 nA for the balanced VMDP with 10 pairs of photodiodes) and a high external quantum efficiency (0.64 A/W). The relative intensity noise (RIN) of a semiconductor distributed feedback laser has been suppressed by 17 dB, and the RF signal has been enhanced by 6 dB. To the authors' knowledge, this is the first report of monolithic distributed balanced photodetectors. The experimental results indicate that the distributed balanced photodetector will have a major impact on most RF photonic systems.

VI. ACKNOWLEDGEMENT

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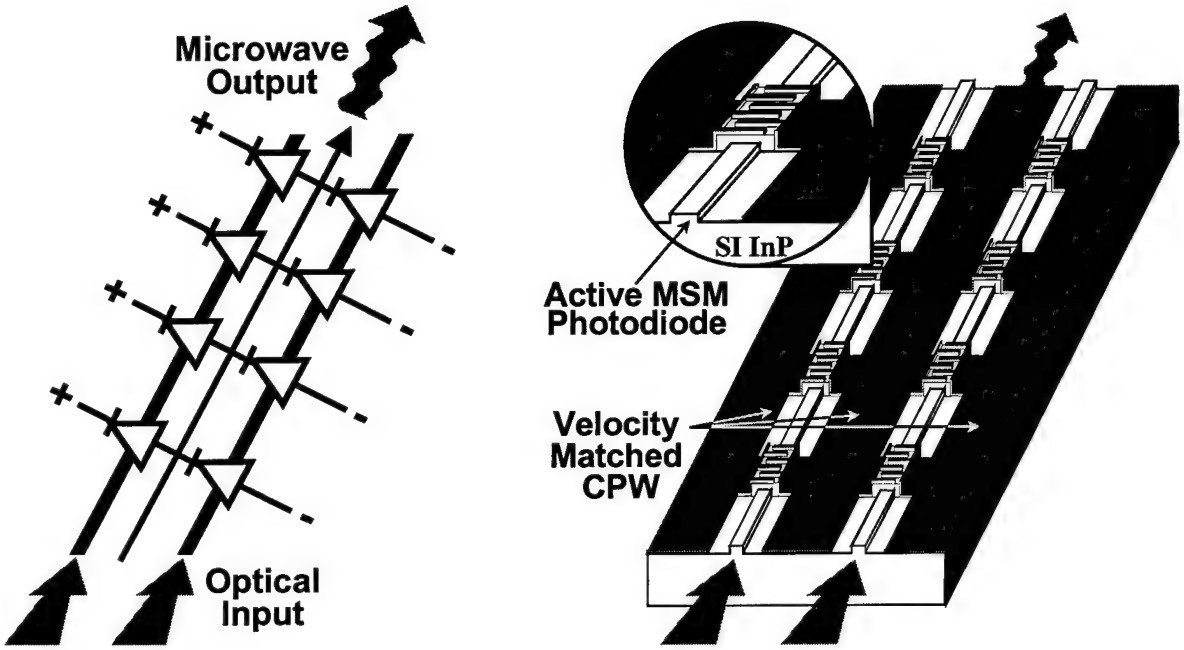
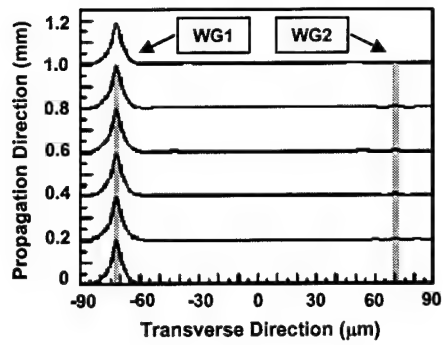
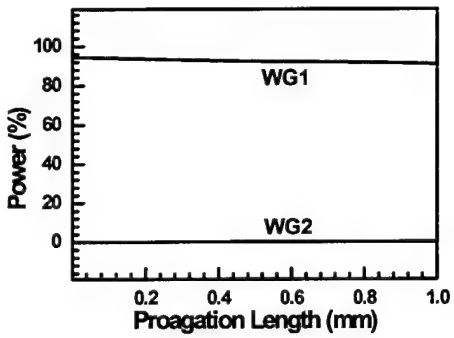


(a) (b)

Figure 1. (a) Principle and (b) schematic structure of the distributed balanced photodetector. The inset shows the active region with an MSM photodiode.



(a)



(b)

Figure 2. (a) Simulated optical field profile and (b) optical power distribution along the waveguides.

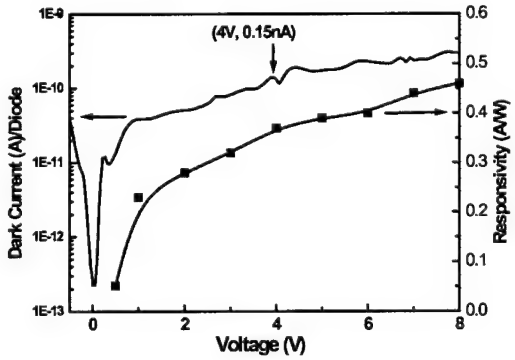


Figure 3. The dark current (left) and the responsivity (right) versus bias voltage for individual VMDP (one array of photodiodes) in the balanced detector. At the operational bias (4 V), the dark current is 0.15 nA.

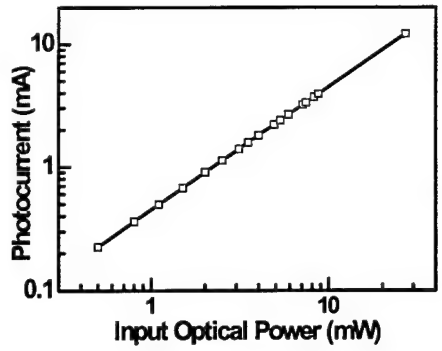


Figure 4. DC photocurrent versus input optical power (without AR coating). The DC photocurrent remains linear up to 12 mA.

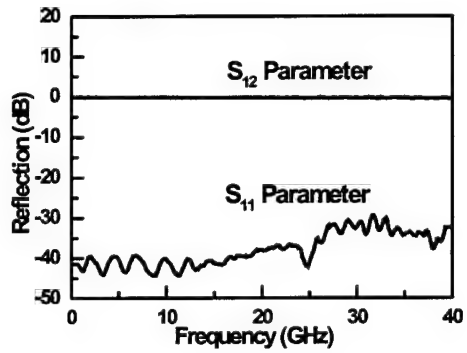


Figure 5. The Measured S parameters of the CPW.

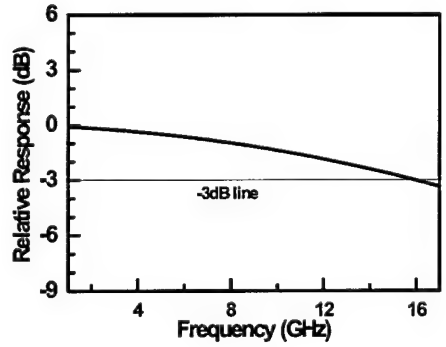


Figure 6. Frequency response of the distributed balanced photodetector with only one waveguide illuminated.

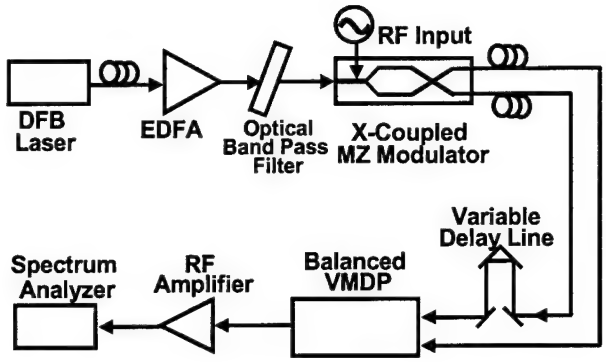


Figure 7. Experimental setup for balanced detection. The complimentary input signals are produced by the X coupled MZ modulator.

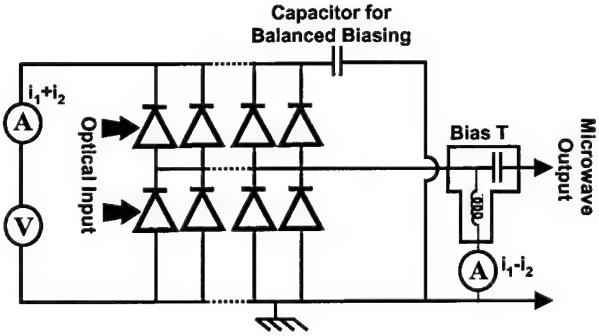


Figure 8. The biasing circuit for balanced detection.

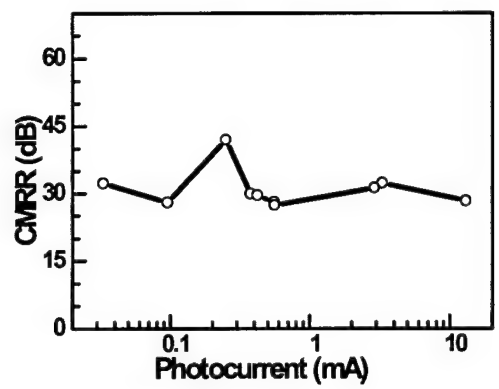


Figure 9. Common mode rejection ratio (CMRR) versus photocurrent for the distributed balanced receiver. The high CMRR results from the closely matched photodiode characteristics in our monolithic device.

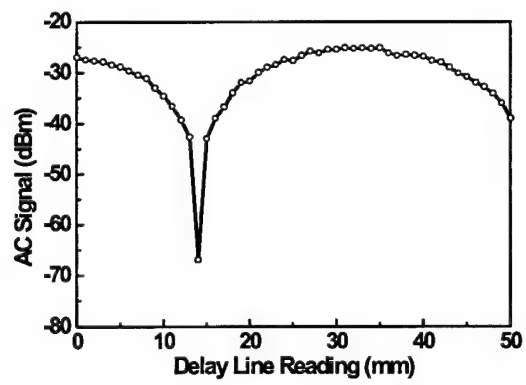


Figure 10. The peak RF power detected in the balanced mode versus the time delay of one input light. Periodic variation is observed. The period is measured to be 38.75 mm at 8 GHz RF signal, which is very close to the theoretical value. The Extinction ratio is greater than 44 dB.

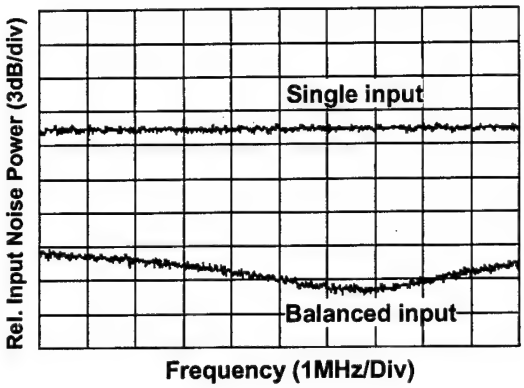


Figure 11. The noise spectra of a DFB laser measured by the distributed balanced photodetector in unbalanced mode (top trace) and balanced mode (bottom trace). Maximum noise cancellation occurs at the frequency at which the RF noise is 180° out of phase.

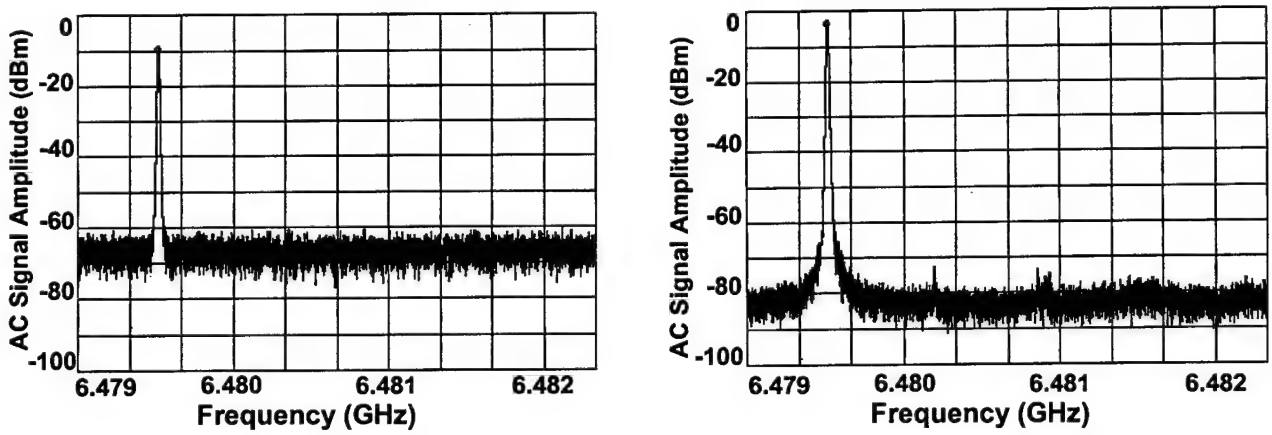


Figure 12. The RF spectra of the modulated signal detected in (a) unbalanced and (b) balanced mode. The peak of the balanced output is 6-dB higher than that of the unbalanced signal. Noise suppression in excess of 17-dB is achieved.

Noise Suppression Properties of Distributed Balanced Photodetectors for High Performance RF Photonic Links

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ABSTRACT

We report on the noise suppression properties of a novel distributed balanced photodetector that we designed and fabricated. Large improvement in signal-to-noise ratio (SNR) has been observed over a wide range of received optical power and RF signal phase mismatch.

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Balanced photodetectors are of great interest to analog fiber optic links because they can suppress relative intensity noise (RIN) of lasers and amplified spontaneous emission noise (ASE) from erbium-doped fiber amplifiers (EDFA). When used in conjunction with an external modulator with complementary outputs, shot noise-limited system performance can be achieved [1]. In order to fully exploit the advantages of the balanced systems, balanced photodetectors with high saturation photocurrents and broad bandwidth are required. Monolithically integrated balanced photodetectors offer superior performance (broader bandwidth, better matching of photodiodes) and reduced packaging cost. However, most of the integrated balanced photodetectors reported to date have low saturation photocurrents and are not suitable for analog applications.

Previously, we have reported a novel distributed balanced photodetector [2]. It integrates two velocity matched distributed photodetectors (VMDP) with a microwave coplanar waveguide (CPW). This new device inherits the basic advantages of the VMDP, namely, broad bandwidth and high saturation photocurrent [3]. In this paper, we reported on the noise suppression properties of the monolithic balanced distributed photodetector. A high signal-to-noise (SNR) and large suppression of the laser RIN over a broad range of input powers has been observed in the RF photonic link employing the balanced VMDP.

Figure 1 shows the schematic of the balanced distributed photodetector. It consists of two input optical waveguides, two arrays of high-speed metal-semiconductor-metal (MSM) photodiodes distributed along the optical waveguides, and a 50Ω coplanar waveguide (CPW) output transmission line. By biasing the photodiodes in balanced mode, only the *difference photocurrents* are collected by the CPW. The balanced VMDP showed a RIN suppression of more than 17 dB with a very good common mode rejection ratio (CMRR) > 27 dB.

An RF photonic link with a dual-output complementary Mach-Zehnder modulator (MZM) has been set up to characterize the noise properties of the distributed balanced receiver. The RF carrier is fixed at 6.5 GHz. Figure 2 shows the SNR of the link versus the received optical power for both the distributed balanced receiver and the reference receiver with a single detector. The SNR for the single detector receiver is almost constant with increasing optical power, indicating that the receiver noise is dominated by the RIN. In contrast, the SNR for the balanced receiver increases monotonically with optical power upto 15 mW. For optical power greater than 15 mW, the SNR still increases monotonically with optical power at a smaller rate. This suggests the presence of some residue RIN. Comparing the two

receivers, it is also noted that the SNR for the balanced receiver is 23 dB higher than the single detector receiver.

The RF signals detected by the balanced detector should be exactly at 180° out of phase for optimum noise suppression. This requires the lengths of the fiber from the complimentary MZM to the detector to be exactly the same in length. In practical applications, the optical path length will drift slightly due to environmental changes and it is important to understand the impact of phase mismatch. Figure 3 plots the variation in the signal peak and the amount of noise suppression when the phase difference of the RF signal at 6.5 GHz deviates from 180°. The measured data shows that even with a phase variation of 100°, our device can suppress more than 9 dB of RIN noise whereas the signal peak reduction was less than 4 dB. As balanced detector amplifies the RF signal by 6dB, with a phase deviation of 100°, the signal is still higher than that of an unbalanced detector. For the RF signal at 6.5 GHz, 100° phase variation between two fibers corresponds to ~8.5mm of fiber length.

In conclusion, we measured the SNR and phase tolerance of the input RF signals of the high power distributed balanced receiver. This monolithic balanced receiver has the potential to dramatically improve the performance of RF photonic links.

Acknowledgment

This project is supported in part by ONR MURI on RF Photonics, National Radio Astronomy Observatory, JESP and UC MICRO.

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[3] L.Y. Lin, M.C. Wu, T. Itoh, T.A. Vang, R.E. Muller, D.L. Sivco, and A.Y. Cho, "Velocity-matched distributed photodetectors with high-saturation power and large bandwidth," *IEEE Photon. Technol. Lett.*, vol. 8, no. 10, pp. 1376 - 1378, 1996.

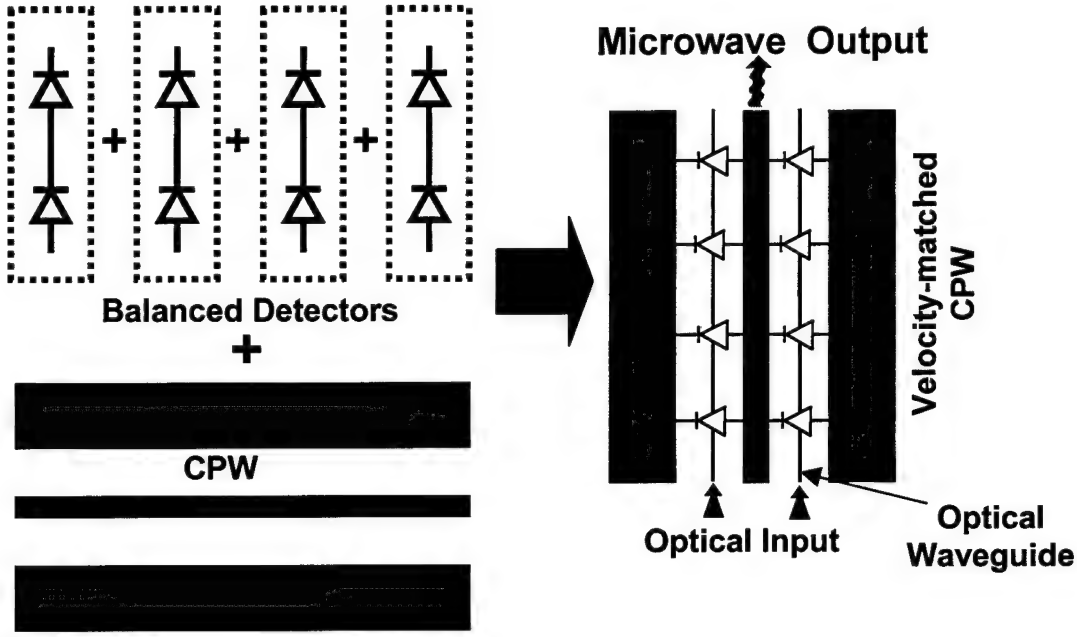

Figure 1. Principle and schematic structure of the distributed balanced photodetector. We cascaded multiple balanced photodetector pairs in series along a coplanar waveguide to increase saturation photocurrent.

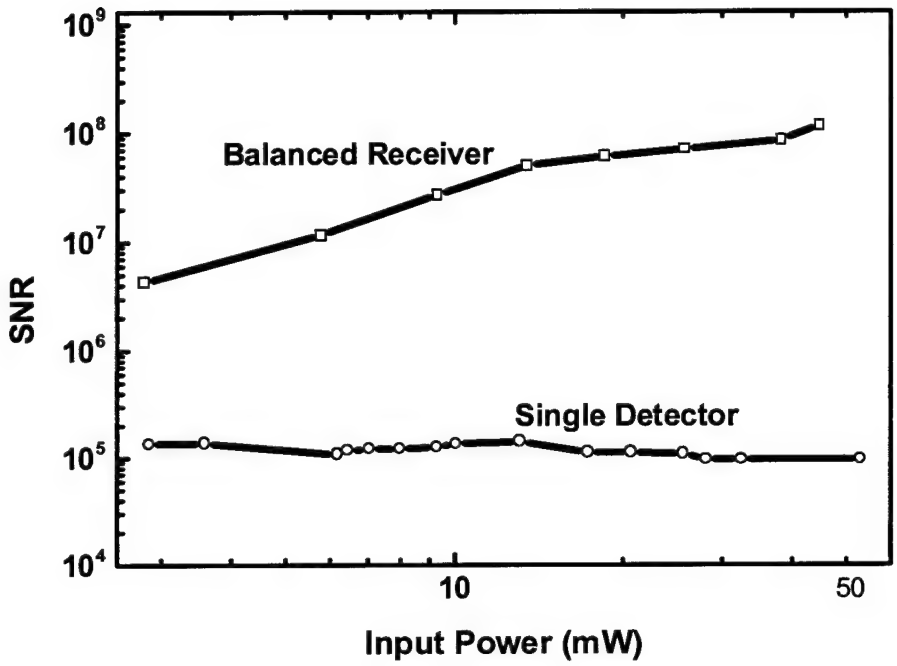

Figure 2. Measured signal-to-noise ratio (SNR) of the balanced receiver. The lower curve shows the SNR for the receiver in unbalanced configuration.

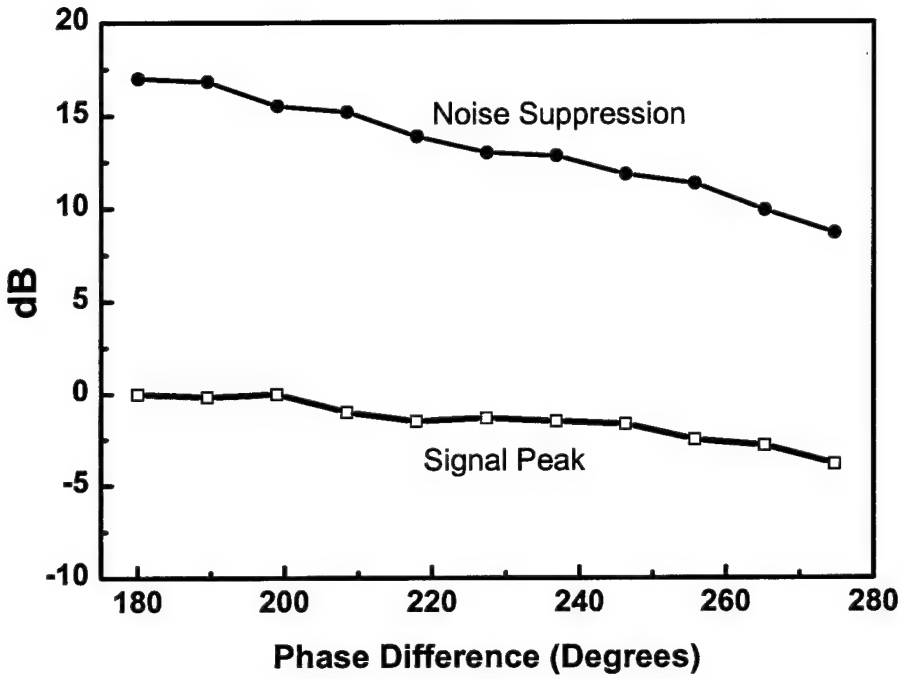

Figure 3. Total amount of noise suppression and the deviation of the signal peak versus phase deviation of the RF signal from 180°. Even with a phase variation of 100°, the receiver can suppress more than 9 dB of RIN noise whereas the signal peak reduction was less than 4dB.

Distributed Balanced Photodetectors for High Performance RF Photonic Links

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ABSTRACT

A novel velocity-matched distributed *balanced* photodetector with a 50Ω coplanar waveguide output transmission line has been experimentally demonstrated in the InP/InGaAs material system. Distributed absorption and velocity matching are employed to achieve high saturation photocurrent. A common mode rejection ratio of 27 dB has been achieved. The RF link experiment conducted at 6.48 GHz shows that the laser intensity noise has been suppressed by more than 17 dB.

INDEX TERMS

RF photonics, noise suppression, analog fiber optic links, balanced photodetectors, optical receivers

Distributed Balanced Photodetectors for High Performance RF Photonic Links

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I. INTRODUCTION

Balanced photodetectors are of great interest to analog fiber optic links because they can suppress laser relative intensity noise (RIN) and amplified spontaneous emission noise (ASE) from erbium-doped fiber amplifiers (EDFA) [1]. Because balanced photodetectors can achieve shot noise-limited link performance, we can continue to improve the noise figure and the spurious-free dynamic range (SFDR) of externally modulated links by increasing the power of the optical carrier. Therefore, balanced photodetectors with broad bandwidth and high saturation photocurrents are particularly important for analog fiber optic link applications. Though discrete balanced photodetectors with high saturation power have been reported, their bandwidth is limited [2]. Most of the reported integrated balanced receivers suffer from low saturation power and are not suitable for analog links. [3-5] Previously, we have reported a velocity-matched distributed photodetector (VMDP) with a peak saturation photocurrent of 56 mA and a 3-dB bandwidth of 49 GHz [6]. Recently, InP-based long wavelength VMDP has also been reported [7]. Compared with other photodetector structures, the VMDP is more suitable for implementing the balanced photodetection since it has separate optical and microwave waveguides. In this

letter, we propose and demonstrate a novel, monolithic distributed balanced photodetector that can simultaneously achieve high saturation photocurrent and large bandwidth. A common mode rejection ratio of 27 dB and a noise suppression of 17dB have been experimentally demonstrated.

II. DESIGN AND FABRICATION

Figure 1 shows the schematic of the distributed balanced photodetector. It consists of two input optical waveguides, two arrays of high-speed metal-semiconductor-metal (MSM) photodiodes distributed along the optical waveguides, and a 50Ω coplanar waveguide (CPW) output transmission line. The diodes are 23 μm long and 5 μm wide. The MSM fingers with 1μm width and 1μm spacing are patterned by optical lithography. The central conductor of the CPW has a width of 55 μm and the separation between the central conductor and the ground conductors is 85 μm. The 10.5 μm overlap of the MSM fingers is designed to provide the required capacitive loading for velocity matching. Unlike previously reported slow-wave CPW [8] that ignored the resistance of the MSM photodiode fingers, finite metal thickness and transmission line discontinuities in their quasi-static calculations, we used a full-wave analysis to achieve the velocity and impedance matching.

The distributed balanced photodetector inherits the basic advantages of the VMDP, namely, high saturation photocurrent, high quantum efficiency and large bandwidth. It should be noted that even though only the difference current (AC signal) is collected in the balanced photodetector, the DC light is still absorbed in the photodiodes. As a result, high DC saturation photocurrent is required for the distributed balanced photodetectors. By coupling only a small fraction of light from the passive waveguide to each individual photodiode, the photodiodes are

kept below saturation even under intense optical input. The bandwidth of the distributed balanced photodetector remains high because of the velocity matching.

Beam propagation method (BPM) simulation was used to investigate the optical properties of the balanced VMDP. The simulation results indicate that there is no crosstalk between the parallel optical waveguides that are 140 μm apart. The simulation also shows that an input beam with TM polarization contributes to the optimum performance and the absorption per photodiode and the optical coupling loss between photodiodes are shown to be 8.8% and 3.2%, respectively for the TM polarization. Our calculation shows that the AC quantum efficiency of 42% can be achieved for balanced receiver with 10 pairs of photodiodes. The optical waveguide consists of the following: a 200-nm-thick $In_{0.52}Al_{0.37}Ga_{0.11}As$ lower cladding layer, a 500-nm-thick $In_{0.52}Al_{0.178}Ga_{0.302}As$ core region, a 200-nm-thick $In_{0.52}Al_{0.37}Ga_{0.11}As$ first upper cladding layer, and a thin $In_{0.52}Al_{0.48}As$ second upper cladding layer. The 150-nm-thick absorption region is located on top of the waveguide for evanescent coupling. Since the Schottky barrier height of most metals on the InGaAs is typically between 0.2-0.3 eV, an $In_{0.52}Al_{0.48}As$ cap layer is used to increase the Schottky barrier height and therefore decrease the dark current in the photodiodes [9,10]. A graded layer is incorporated in the structure to reduce the minority carrier trapping at the InAlAs-InGaAs band edge discontinuity.

Fabrication of the receiver started with removing the InGaAs layer except in the active areas of the photodiodes. Ridge waveguides with 100 nm ridge height were formed by wet chemical etching. The active regions of the photodiodes were defined by opening 6μm ×23 μm windows on the 150-nm-thick silicon nitride (Si_3N_4) film deposited by plasma-enhanced

chemical vapor deposition (PECVD). Buffered HF was used to remove the Si_3N_4 in the windows. The Ti-Au electrodes and contact pads of the MSM photodiodes were then delineated by standard lift-off processes. The tips of the MSM fingers are placed on top of Si_3N_4 to suppress the soft breakdown and enables the MSM diodes to operate over a wider range of bias voltage [11]. A 350-nm-thick coplanar waveguide was formed by standard lift-off process to connect the distributed balanced photodetectors. By measuring the forward current-voltage characteristics, the barrier height of the metal-semiconductor junction was estimated to be 0.57 eV.

III. MEASUREMENTS AND DISCUSSIONS

The balanced VMDP exhibits very good electrical and optical characteristics. The dark current is measured to be 28μA/cm^2 at 10V bias, the lowest reported for InAlAs/InGaAs MSM photodiodes. By coupling light directly from a lensed fiber, the average DC responsivity (15 devices tested) was measured to be 0.45A/W at 8V bias. Responsivity as high as 0.6A/W has been observed in some devices. The photo response of a laser beam with TM polarization is measured to be ~3 dB higher than that of TE polarization. The coupling efficiency of the lensed fibers in our setup was calculated to be ~50 %. With antireflection (AR) coating to the balanced receiver facet (30% Fresnel loss), the average responsivity can be increased to 0.64A/W. The responsivity can be further improved by optimizing the coupling efficiency of the lensed fiber as well as reducing the coupling loss between the passive and active waveguide regions by better controlling the etching steps in the fabrication.

An HP 8510C network analyzer was used to measure the characteristic impedance and the microwave return loss (S_{11}) of the balanced receiver. The characteristic impedance of the

receiver is very well matched to 50Ω. The S_{11} is as low as -30 dB from 45MHz to 40GHz. The CPW has very low insertion loss. The measured S_{12} shows a drop of only 0.6dB from 45MHz to 40 GHz.

The frequency response of the balanced VMDP was first characterized with light coupled to one waveguide only. Using the optical heterodyne technique with two external cavity tunable semiconductor lasers at 1.55 μm, the 3-dB bandwidth was found to be 16 GHz for both photodetector arrays. The bandwidth is currently limited by the carrier transit time of the MSM photodiodes. Since our bandwidth of the capacitance loaded CPW is much greater than 40 GHz, the bandwidth of the balanced VMDP can be increased by scaling down the MSM photodiodes. Theoretical simulation indicates that bandwidth > 100 GHz is achievable.

Figure 2(a) depicts the experimental setup for balanced detection. A distributed feedback (DFB) laser with 1542-nm wavelength and 0 dBm output power is employed as optical source. It is amplified by an EDFA and then filtered by an optical bandpass filter with 2-nm bandwidth. The microwave signal was modulated onto the optical carrier by an X-coupled Mach-Zehnder modulator (MZM), which produces two complementary outputs for the balanced VMDP. The outputs are coupled to the balanced VMDP by two lensed fibers. To maximize the signal enhancement and noise cancellation, it is important to match the amplitudes and phases of the two detected microwave signals. In our experiment, a variable attenuator was used to match the amplitudes of the photocurrents. Typical balance between the VMDP was within 2% of the total photocurrent reading, which was limited to 4 mA in our current experiments. Since the accuracy of cutting optical fiber lengths is about 1 mm, a variable delay line was used to ensure equal

optical path lengths between the two fibers, which is necessary to produce the broadband 180° out-of-phase RF signals for balanced VMDP. The output from the balanced VMDP was measured using a spectrum analyzer. A common mode rejection ratio of -27dB has been achieved.

Balanced detection is achieved by applying a bias of 8V between the two ground electrodes of the CPW. A custom-made high-frequency probe with an integrated DC-blocking capacitor on one ground probe is used to collect the microwave output signal. The DC difference photocurrent is monitored through the bias-T connected to the probe. To verify the balanced detection, we modulated the optical input at 8-GHz and varied the delay of the fiber optic delay line from 0 to 50 mm. Figure 2(b) shows the RF signal versus the delay. When the RF signals have 0° phase difference, the AC output is cancelled in balanced mode. At 180° phase difference, the RF signal is amplified, the extinction ration is more than 44 dB.

Figure 3 shows the RF spectrum of the output from the balanced VMDP in the unbalanced (only one waveguide is illuminated) and the balanced mode. Suppression of the noise floor by 17-dB has been observed in the balanced mode over a wide frequency range from 6 to 15 GHz. The signal is also enhanced by 6-dB. For bandwidths lower than 6 GHz, the fiber length for one RF period is longer than 50 mm, the maximum delay length in our current setup. We are currently working on a new setup with two fiber optic delay lines to achieve exactly equal optical path lengths for broad band operation without any tuning of the delay line. This will allow us to measure the broadband characteristics of the device in the balanced mode.

IV. CONCLUSION

We have successfully designed, fabricated, and experimentally demonstrated a balanced velocity-matched distributed photodetector (VMDP) with both impedance and velocity matching. The device exhibits a very low dark current and a high external quantum efficiency of 0.64 A/W. Using the balanced VMDP, the relative laser intensity noise (RIN) and the erbium-doped fiber amplifier (EDFA)-added noise have been suppressed by 17-dB, and the RF signal has been enhanced by 6-dB. This was the first integration of balanced detectors with high-power, high-speed distributed photodetectors for high performance RF photonic links.

V. ACKNOWLEDGMENT

The authors would like to acknowledge Dr. D.T.K. Tong of Lucent Technologies-Bell Laboratories for his helpful suggestion about the experimental setup and Dr X. J. Meng of UCLA for his helpful discussion about the measurements. This project is supported by ONR MURI on RF Photonics, National Radio Astronomy Observatory (NRAO), JESP and UC MICRO.

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Figure Captions:

Fig. 1 (a) Schematic structure of the distributed balanced photodetector. The inset shows the active region with an MSM photodiode. (b) The photodiodes connected to the optical waveguide in balanced detection mode.

Fig. 2 (a) Balanced detection setup. The complimentary input signals are produced by the X-coupled MZ modulator. (b) Peak power of AC signal in balanced mode versus the delay. For RF signal at 8 GHz, the period was measured to be 38.75 mm, which is very close to the theoretical value. The power difference between 0° and 180° phase difference is more than 44 dB.

Fig. 3 The AC signal in unbalanced and balanced detection modes are plotted. The balanced output is almost 6-dB higher in amplitude than the unbalanced signal. Noise suppression of greater than 17-dB is achieved.

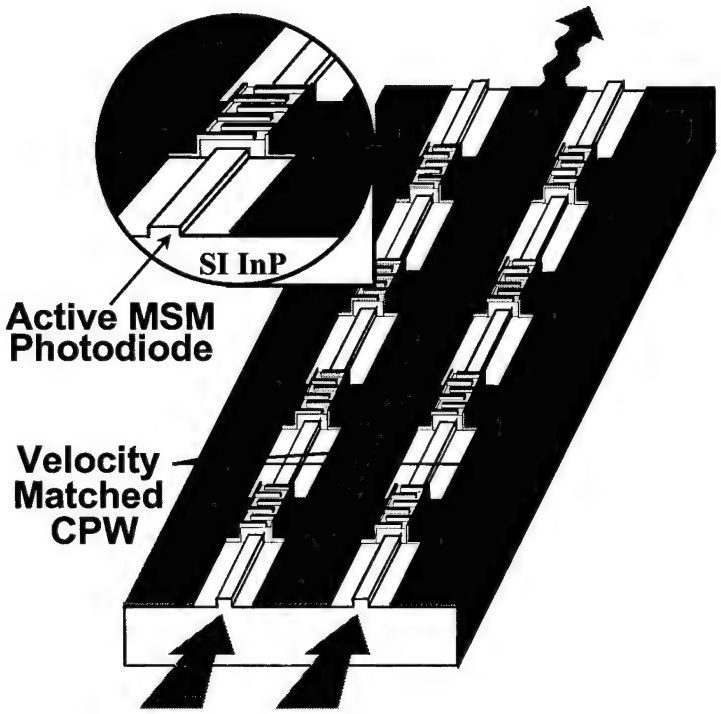

Figure 1(a)

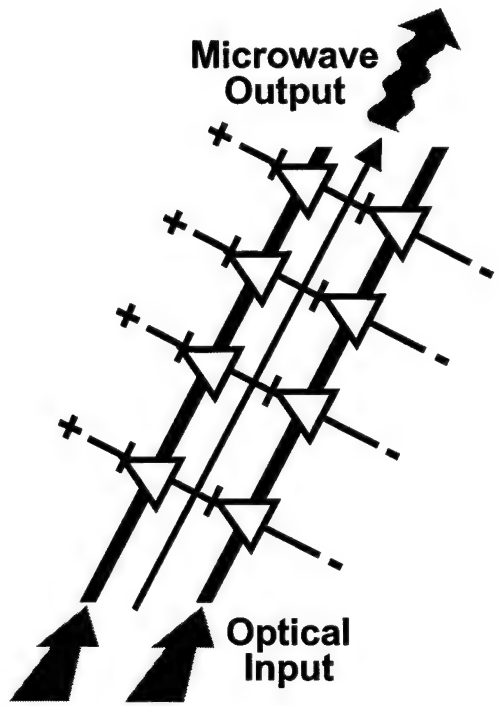

Figure 1(b)

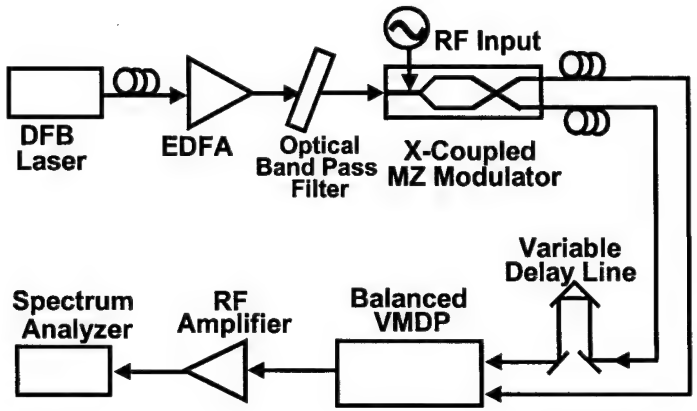
RF Input
DFB
Laser
EDFA
Optical
Band Pass
Filter
X-Coupled
MZ Modulator
Variable
Delay Line
Spectrum
Analyzer
RF
Amplifier
Balanced
VMDP

Figure 2 (a)

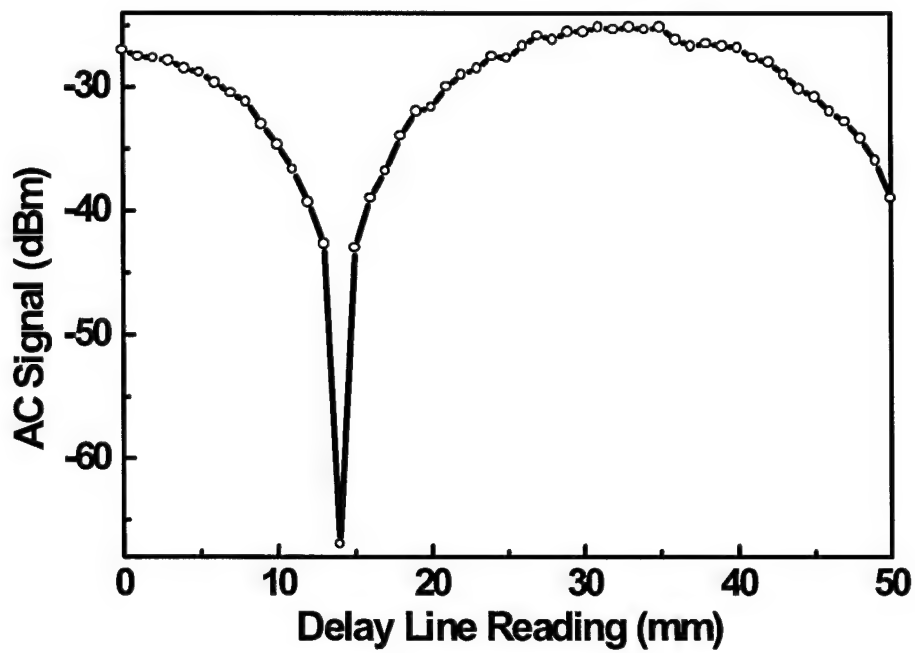

Figure 2(b)

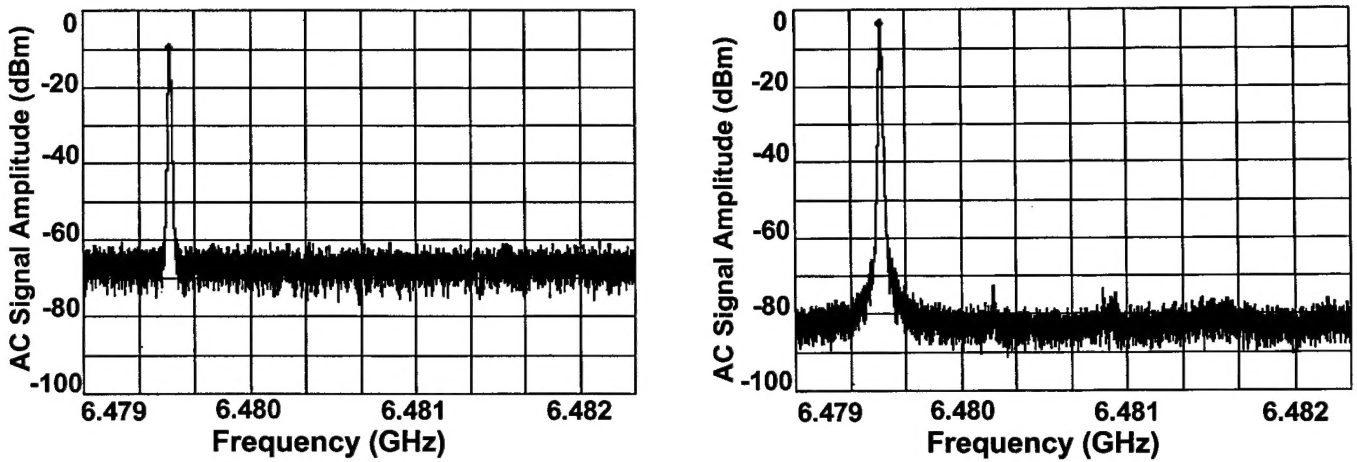
AC Signal Amplitude (dBm)
0
-20
-40
-60
-80
-100
6.479
6.480
6.481
6.482
Frequency (GHz)
AC Signal Amplitude (dBm)
0
-20
-40
-60
-80
-100
6.479
6.480
6.481
6.482
Frequency (GHz)

Figure 3

Distributed Balanced Photodetectors for High Performance RF Photonic Links

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Balanced photodetectors are of great interest to analog fiber optic links because they can suppress laser relative intensity noise (RIN) and amplified spontaneous emission noise (ASE) from erbium-doped fiber amplifiers (EDFA) [1]. Because balanced photodetectors can achieve shot noise-limited link performance, the noise figure and spurious-free dynamic range of the link continue to be improved by increasing the power of the optical carrier. Therefore, balanced photodetectors with broad bandwidth and high saturation photocurrents are particularly important for analog fiber optic link applications. Previously, we have reported a velocity-matched distributed photodetector (VMDP) with a peak saturation photocurrent of 56 mA and a 3-dB bandwidth of 49 GHz [2]. Compared with other photodetector structures, the VMDP is more suitable for implementing the balanced photodetection since it has separate optical and microwave waveguides. Here, we demonstrate a novel distributed balanced photodetector that can achieve high saturation photocurrent and large bandwidth simultaneously. A 3-dB frequency of 16 GHz and a responsivity of 0.64 A/W have been achieved.

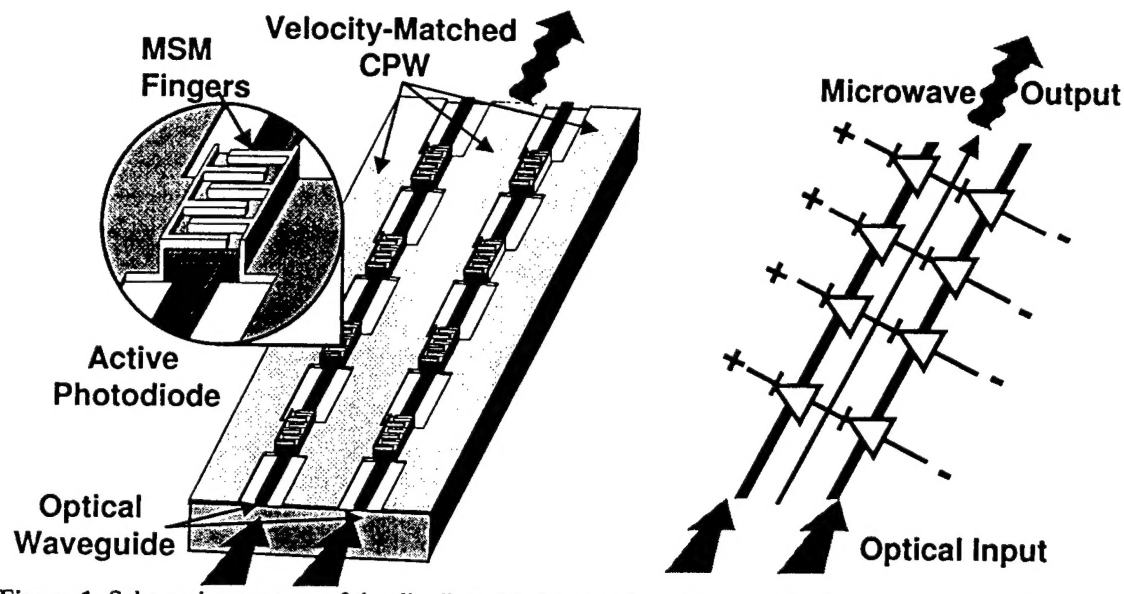

Figure 1. Schematic structure of the distributed balanced photodetector. The inset shows the active region with an MSM photodiode. Figure on the right shows the photodiodes connected to the optical waveguide in balanced detection mode.

Figure 1 shows the schematic of the balanced distributed photodetector. It consists of two input optical waveguides, two arrays of high-speed metal-semiconductor-metal (MSM) photodiodes distributed along the optical waveguides, and a 50Ω coplanar waveguide (CPW) output transmission line. Beam propagation simulation results indicate no crosstalk between the parallel optical waveguides, and the absorption per photodiode and the optical coupling loss between photodiodes are 8.8% and 3.2%, respectively. The diodes are 23 μm long and 5 μm wide. The MSM fingers are patterned by optical lithography. The central conductor of the CPW has a width of 55 μm and the separation between the central conductor and the ground conductors is 85 μm. The finger overlap of 10.5 μm is designed to provide the required capacitance loading for velocity matching. The matching ensures broadband operation. Unlike previously reported slow-wave CPW [3] that ignored the resistance of the MSM photodiode

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out-of-phase RF signals for balanced VMDP. The output from the balanced VMDP was measured using a spectrum analyzer.

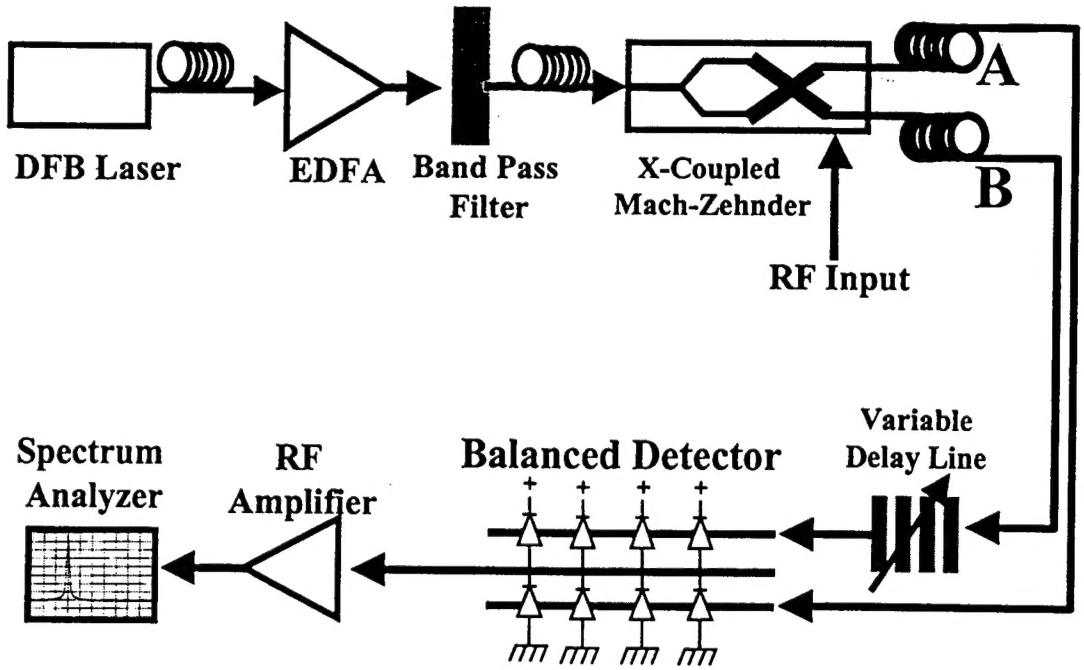
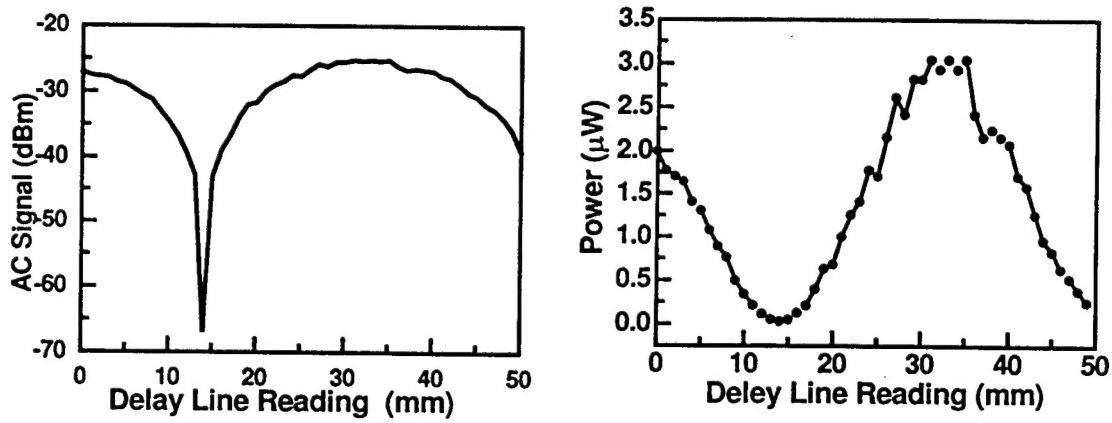


Figure 3. Balanced detection setup. The complimentary input signals are produced by the X-coupled MZ modulator.

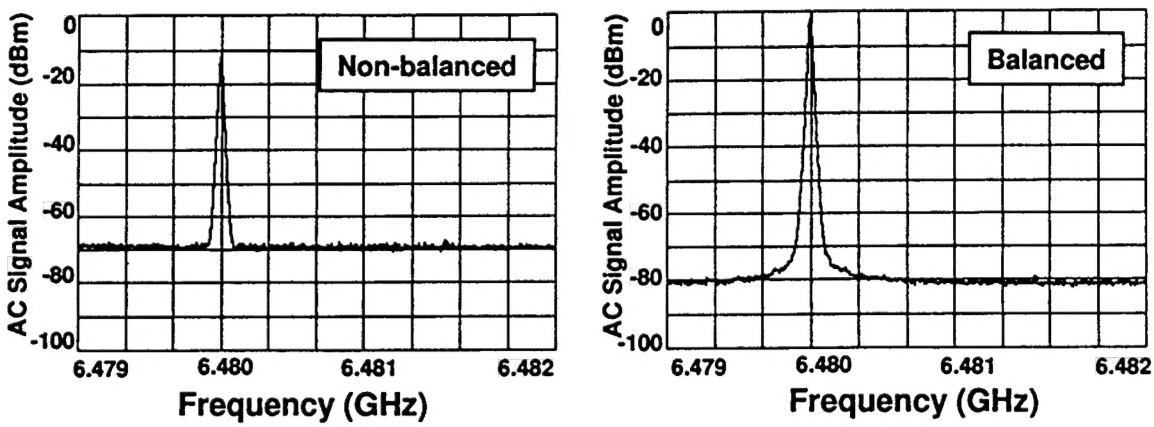
The device was biased in balanced mode by biasing one of the ground electrodes of the CPW at 8Volts. We used a custom made probe with integrated DC-blocking capacitor on the ground that connects to the CPW ground biased at higher voltage. To verify the balanced detection, we modulated the optical input at 8GHz and tuned the fiber optic delay line from 0 to 5mm delay. Figure 4 shows the RF signal verses the delay. When the RF signals have 0° phase difference, the AC output is cancelled in balanced mode. At 180° phase difference, the RF signal is amplified, the extinction ration is more than 44dB.



(a) (b)

Figure 4. (a) Peak power of AC signal in balanced mode versus the delay. For RF signal at 8 GHz, the period was measured to be 38.75 mm, which is very close to the theoretical value. The power difference between 0° and 180° phase difference is more than 44-dB. (b) The same plot in linear scale.

Figure 5 shows the RF spectrum of the output from the balanced VMDP in the non-balanced (only one waveguide is illuminated) and balanced mode. Suppression of the noise floor by 12-dB has been observed in the balanced mode over a wide frequency range from 6 to 15 GHz. The signal is also enhanced by 6-dB. Typical balance between the VMDP was within 2% of the total photocurrent reading, which was limited to 2 mA in our preliminary experiments. For bandwidths lower than 6 GHz, the fiber length for one RF period is longer than 5 mm, the maximum delay length in our current setup. We are currently working on a new setup with two fiber delay lines to achieve exactly equal optical path lengths for broad band operation without any tuning of the delay line. This will allow us to measure the AC responsivity of the device in balanced mode.



(a) (b)

Figure 5. The AC signal in non-balanced (a) and balanced (b) detection modes are plotted separately. The balanced output is almost 6-dB higher in amplitude than the non-balanced signal. Preliminary results show a noise suppression level greater than 12-dB.

In conclusion, a balanced velocity-matched distributed photodetector (VMDP) with both impedance and velocity matching has been designed and successfully fabricated. Preliminary experimental results shows that the relative intensity noise has been suppressed by 12-dB, and the signal has been enhanced by 6-dB. This was the first integration of high power and high speed balanced detectors with a slow microwave transmission line to be used in high performance RF photonic links.

Acknowledgment

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Reference:

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